2009 International Microwave Symposium

Workshop
WSB

Self-Referenced CMOS Oscillators

Workshop on "Current and Future Trends in Frequency Generation Circuits"

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IEEE

MTT-S

Outline

- Introduction
- Emerging silicon frequency generators
- Self-referenced CMOS oscillators
- Performance benchmarking
- Applications, future trends and conclusion

INTRODUCTION

Section outline

- A brief history of frequency generation
- Typical reference frequencies
- Quartz crystal manufacturing
- Market trends
- Silicon frequency references

Crystal oscillators

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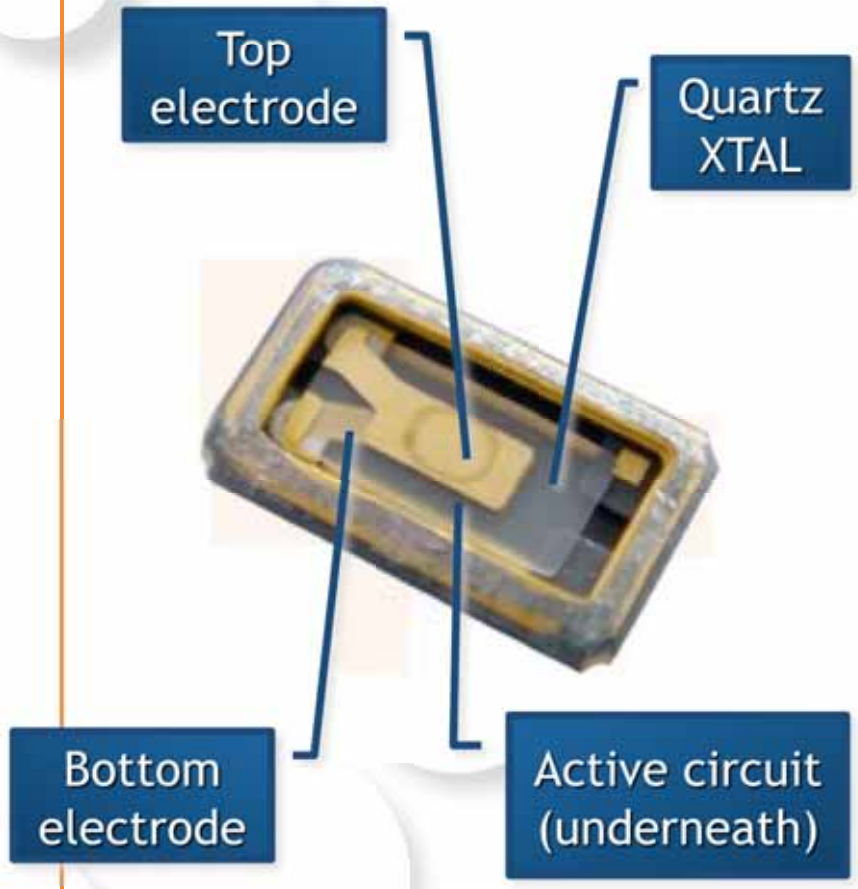
A Modern XO

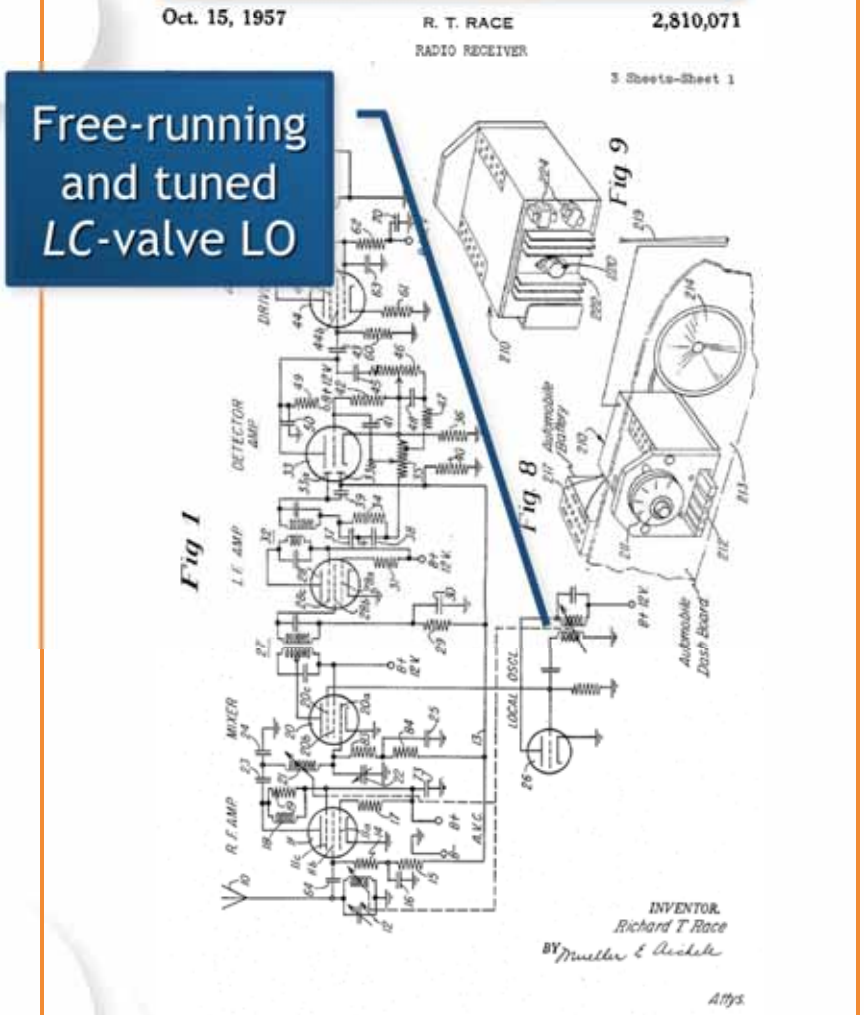


Timeline

- **1880**: piezoelectricity discovered by the Curies
- **1917**: XTAL resonance explored by Langevin for SONAR
- **1919**: frequency control using XTALs by Nicholson and Cady
- **1919 – present**: XOs proliferate; billions of units distributed annually

LC-vacuum tube oscillators

Motorola Radio



Free-running and tuned *LC*-valve LO

Timeline

- **1883**: Edison stumbles across what becomes known as the Edison effect
- **1904**: Fleming patents the oscillation valve using the Edison effect
- **1906 – 1970**: high frequency *LC* vacuum tube oscillators dominate radios

Phase-locked frequency synthesis

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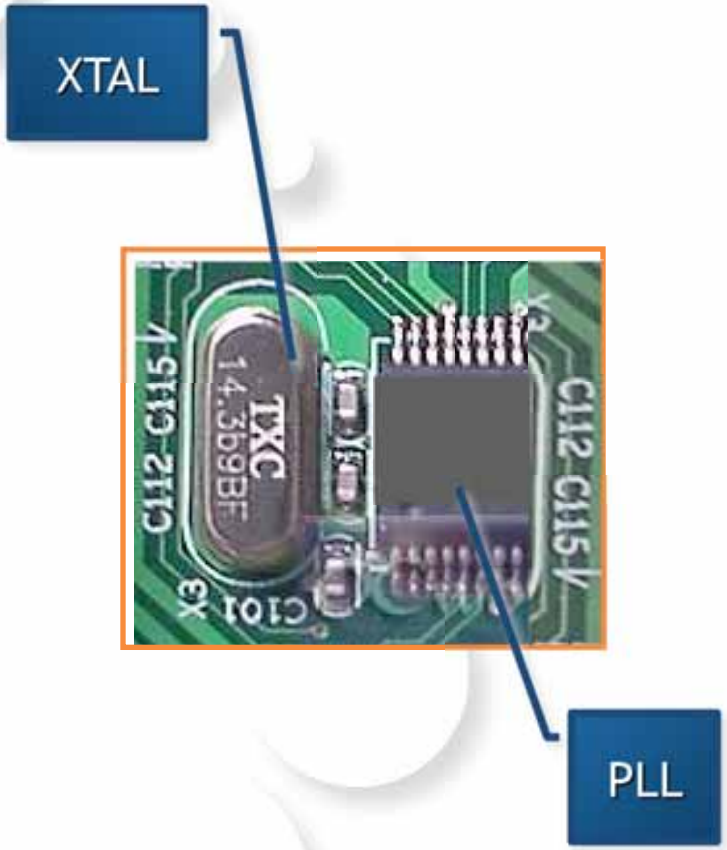
Modern Silicon PLL



Timeline

- **1932**: phase locking introduced by H. de Bellescise, "La Réception Synchrone," Onde Electrique, vol. 11
- **1947**: Transistor invented at Bell Labs
- **1952**: *TI* demonstrates the first transistor radio
- **1969**: Grebene and Camenzind, "Phase Locking As A New Approach For Tuned Integrated Circuits," ISSCC
- **1980s – present**: XTALs + PLLs become the de facto frequency source in microelectronics

Typical wireline reference frequencies

- Protocol (Application): Rate ± Required Accuracy
  - CAN/LinBus (Auto): ~kHz ±1500ppm – ±15kppm
  - USB 2.0 (PC and CE): 48MHz ±500ppm
  - SATA Gen. 1 – Gen. 3 (HDD): 25MHz ±350ppm
  - PCI/PCIe (PC): 33/66MHz ±300ppm
  - Firewire/IEEE1394 (PC and CE): 49.152MHz ±100ppm
  - 1G Ethernet (Data com.): 25MHz ±100ppm
- Observations
  - Rates are <100MHz
  - Fundamental physical limit to XTAL frequency based on geometry
  - Most accuracy requirements > ±100ppm

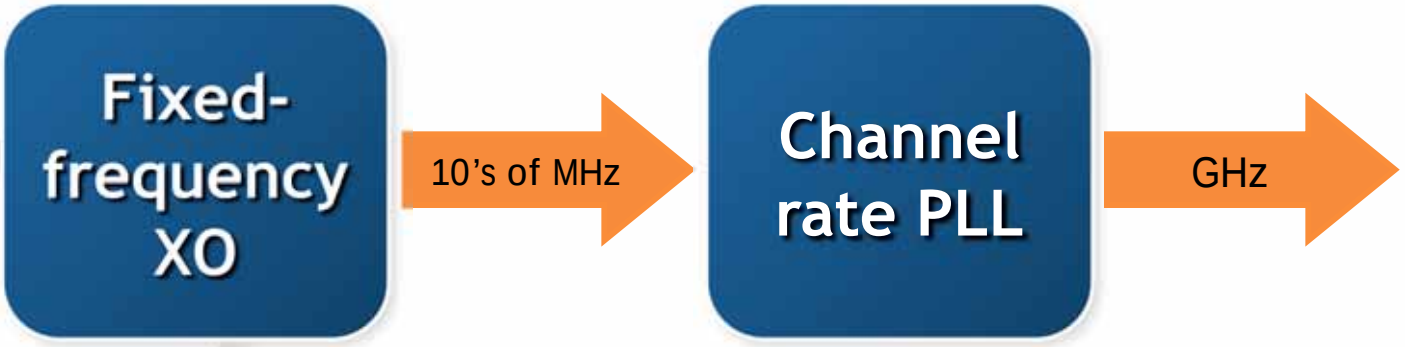
Typical wireless reference frequencies

- Protocol (Application): Freq. ± Required Accuracy
  - Bluetooth, Zigbee (Network radios): 20MHz ±25ppm
  - GSM, etc. (Cellular radios): 13MHz ±5ppm
  - ASK TPMS (Auto): 9.838MHz ±238ppm
- Observations
  - Most frequencies <20MHz
  - Most accuracy requirements <±25ppm
  - Narrowband communications: accuracy must be high
  - Wideband communications: accuracy relaxed

General observations

- Wireline applications require:
  - >±100ppm at <100MHz
- RF applications:
  - <±25ppm at <50MHz
- Standard frequency synthesis
  - Low-frequency XTAL
  - High-frequency channel-rate PLL
  - Often PLLs are used to boost the reference frequency to the channel-rate PLL

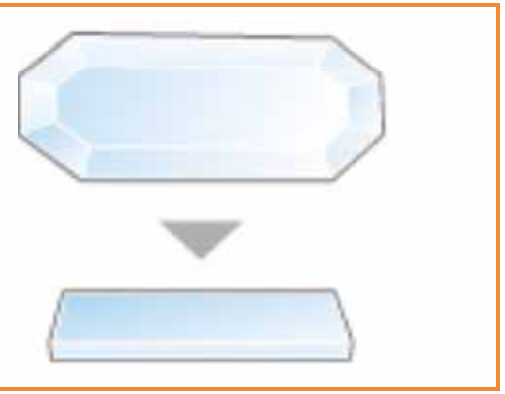
Typical frequency generation



Quartz crystal growth

Wash natural quartz fragments

Process seed crystals



Solvent preparation

Alkaline solution

NaOH

Na_2CO_3

Courtesy of Epson Toyocom: *http://www.epsontoyocom.co.jp/english/special/crystal/enjoy/plant/crystal.html*

Quartz crystal growth

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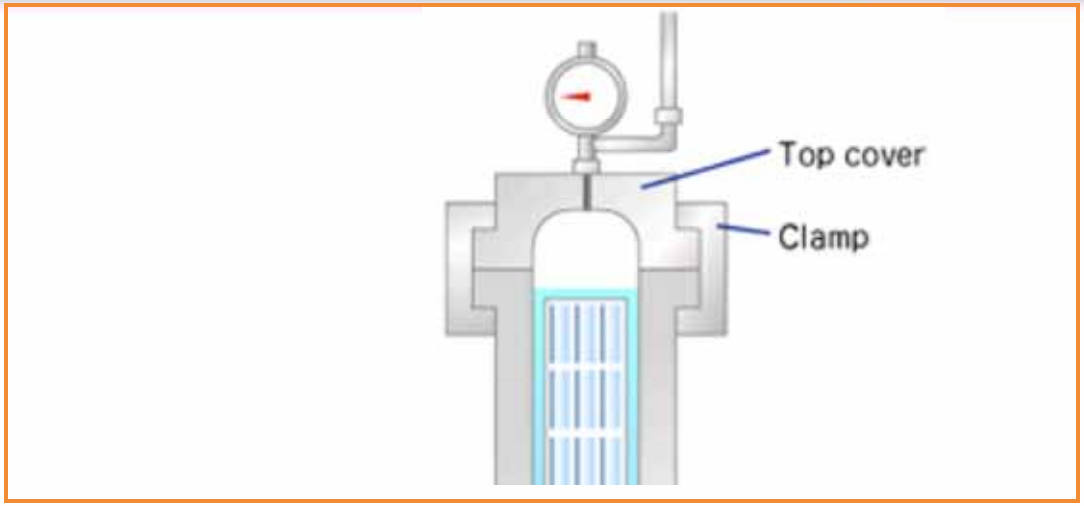
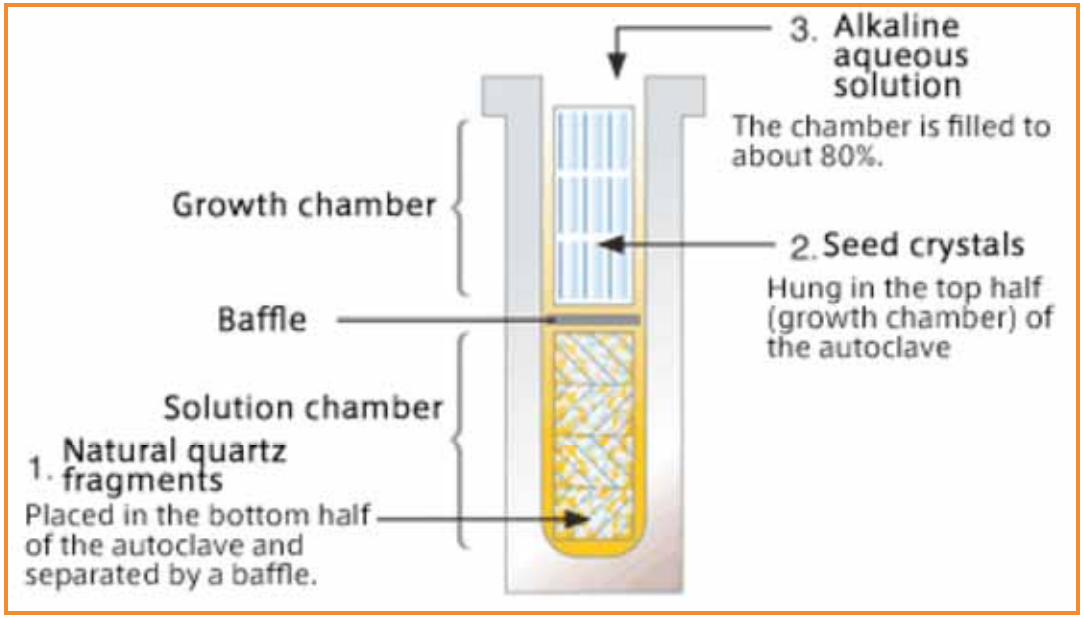
Sealing



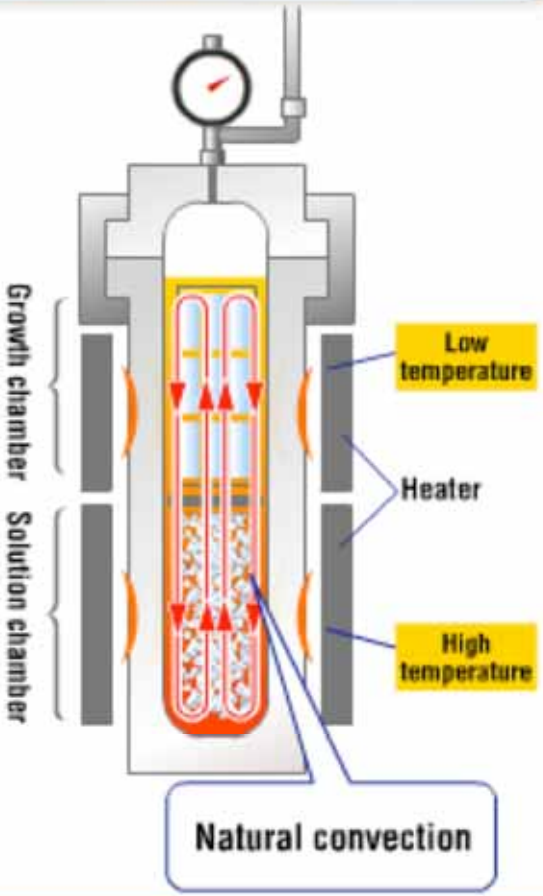
Autoclave preparation



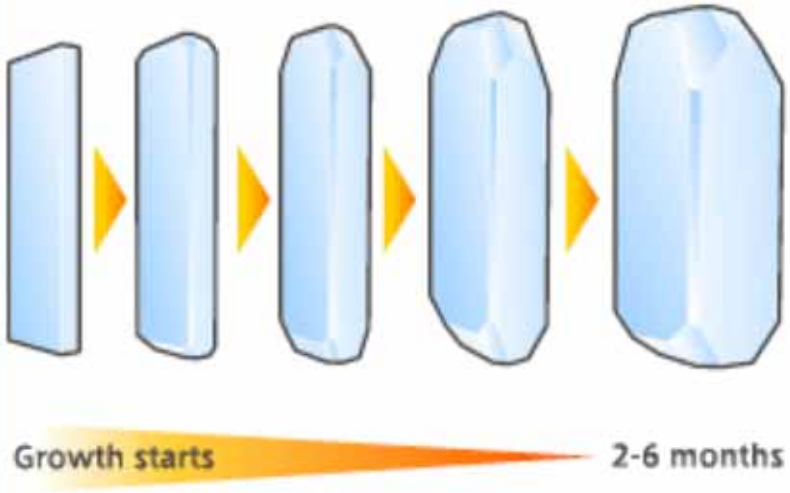
Courtesy of Epson Toyocom: *http://www.epsontoyocom.co.jp/english/special/crystal/enjoy/plant/crystal.html*

Quartz crystal growth

Autoclave heating



Growth



Courtesy of Epson Toyocom: *http://www.epsontoyocom.co.jp/english/special/crystal/enjoy/plant/crystal.html*

Crystal unit manufacturing

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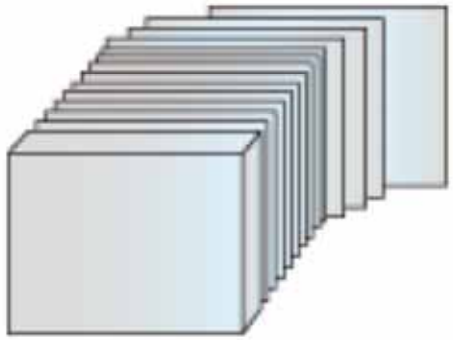
From rough synthetic crystal to block cutting

Wafer slicing



Wafer polishing

Lapping
Surface hills and valleys are removed with a grinding fluid

Etching
The wafer surface is etched to remove roughness

Polishing
The wafer is polished to a mirror finish with an abrasive compound

Courtesy of Epson Toyocom: *http://www.epsontoyocom.co.jp/english/special/crystal/enjoy/plant//timing.html*

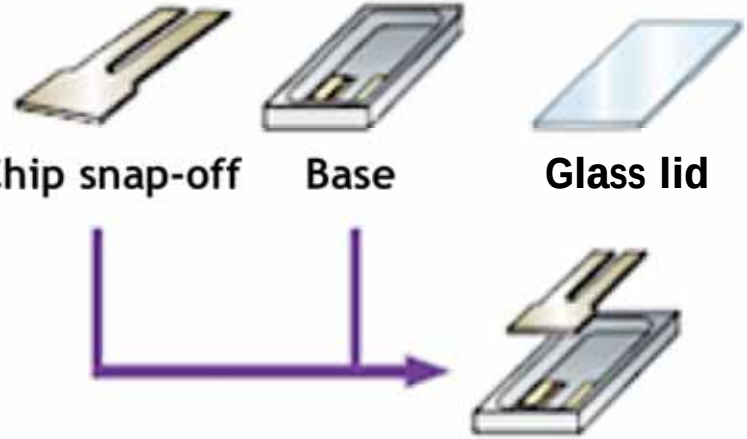
Crystal unit manufacturing

Photoetching

Sputtering
The wafer is coated with gold and chrome

Contour etching
The gold and chrome is removed

Mounting



Courtesy of Epson Toyocom: *http://www.epsontoyocom.co.jp/english/special/crystal/enjoy/plant//timing.html*

Crystal unit manufacturing

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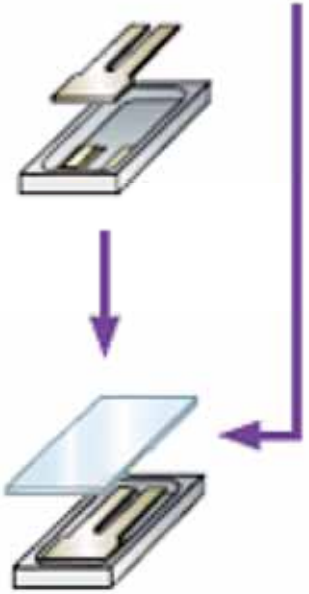
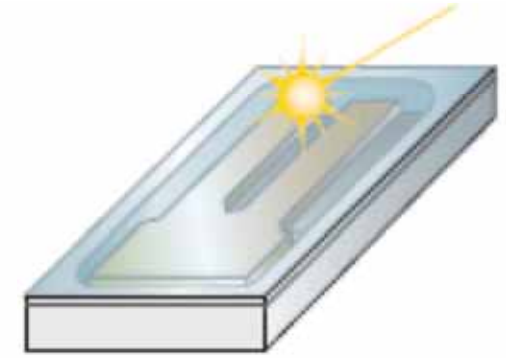
Lid and vacuum sealing

Glass lid



Laser frequency adjusting and marking



Courtesy of Epson Toyocom: *http://www.epsontoyocom.co.jp/english/special/crystal/enjoy/plant//timing.html*

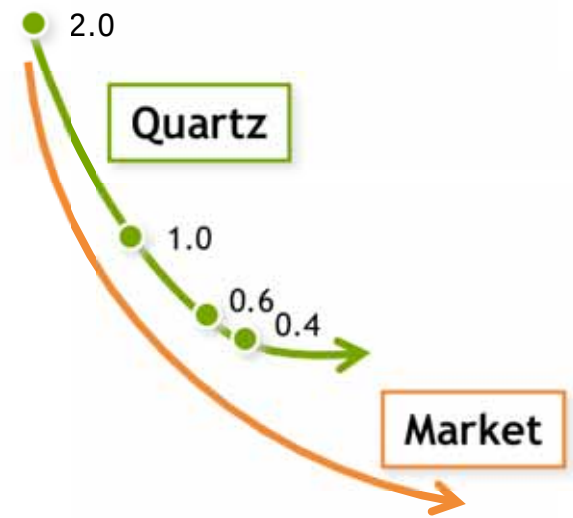
So is there a problem?

- Manufacturing
  - ***Pro***: cost effective through economies of scale
  - ***Con***: 2-6 months for crystal growth alone; manufacturing line required for each individual frequency
- Scalability
  - ***Pro***: size and frequency have scaled historically
  - ***Con***: limits to scaling are imminent
- Functionality and performance
  - ***Pro***: quartz is a ***very*** stable frequency reference
  - ***Con***: quartz is a rock; ckts are required for functionality

Market trends in timing

Market Trends

Increasing Frequency (MHz)	Decreasing Size (mm)	Greater Integration and Functionality

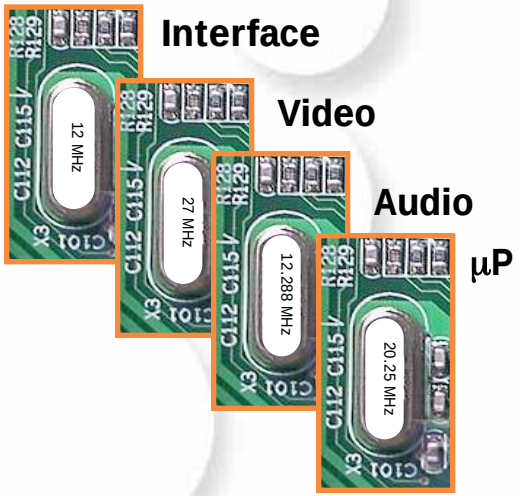


Reducing quartz content

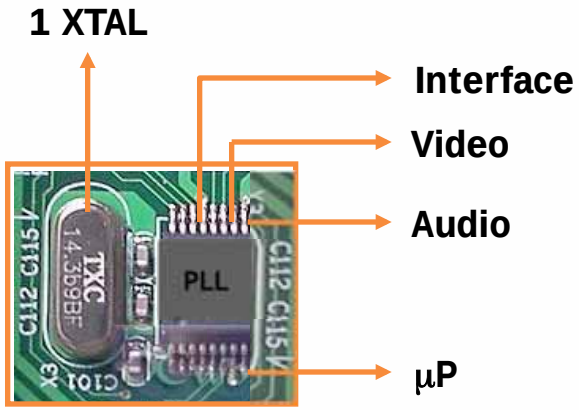
Silicon (CMOS) Frequency Synthesizers

- 1 XTAL for multiple output frequencies via PLLs
- Degraded noise performance due to PLL VCO
- Reduces cost and form-factor
- Increases frequency, flexibility and functionality

Pre 1980's



1980's - Present



Replacing quartz altogether

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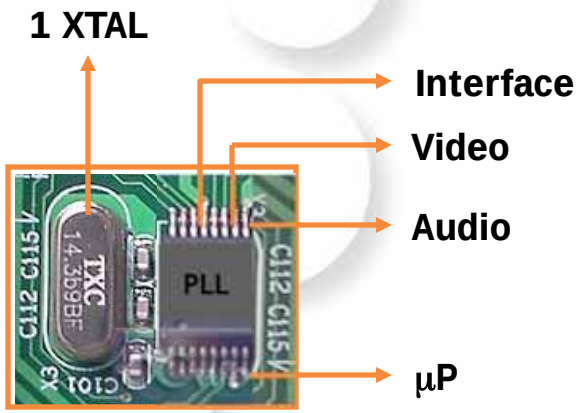
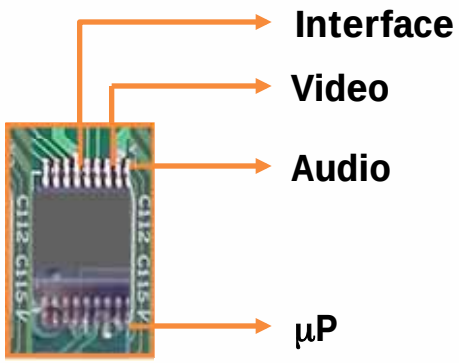
All-Silicon Frequency Synthesizers

- No crystal reference
- Self-contained, self-referenced silicon frequency sources
- Can it be done? And with what technology?
- How would it perform? Could it really rival quartz?

Present



Future?



EMERGING SILICON FREQUENCY GENERATORS

Section outline

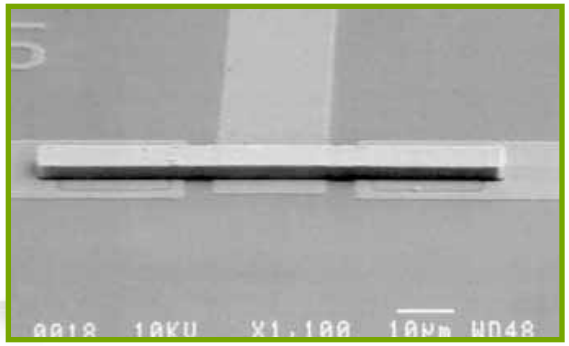
- Key challenges
- MEMS-referenced PLLs
  - *Discera*
  - *SiTime*
- Self-referenced CMOS oscillators
  - *Mobius Microsystems*
  - *Silicon Laboratories*

Key challenges

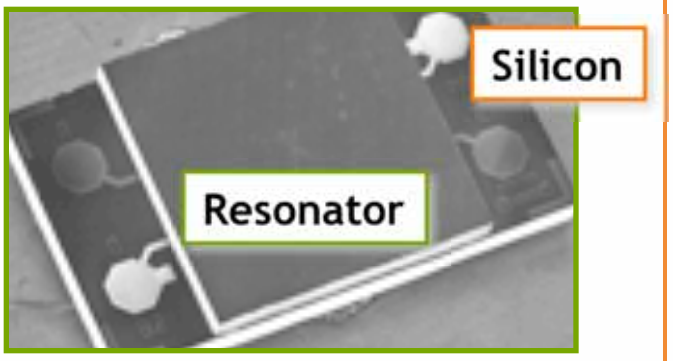
- Quartz is a high-*Q* reference
  - Low jitter and low phase noise are “free”
  - Low power is “free”
- Quartz is stable
  - Low TC depending on cut/mode (e.g. AT/BAW)
  - Environmentally robust
- Quartz is inexpensive
  - Economies of scale make AT/BAW XTALs ~$0.10
- A rival tech. will need to compete with this

Emerging MEMS technologies

Discera

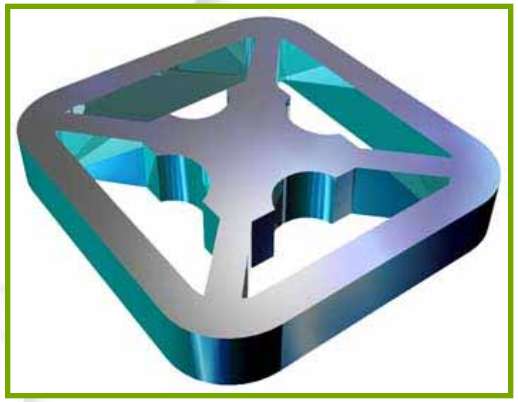


High-Q MHz MEMS resonator

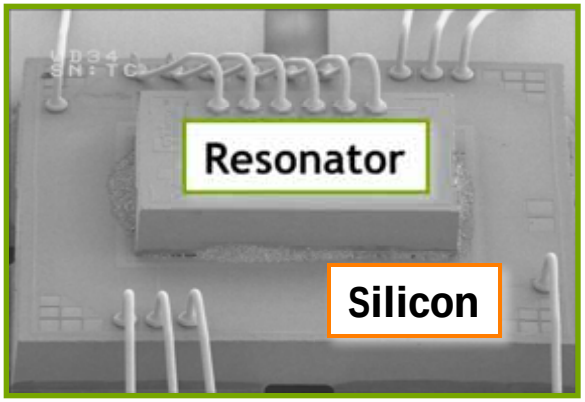


Packaged device

SiTime

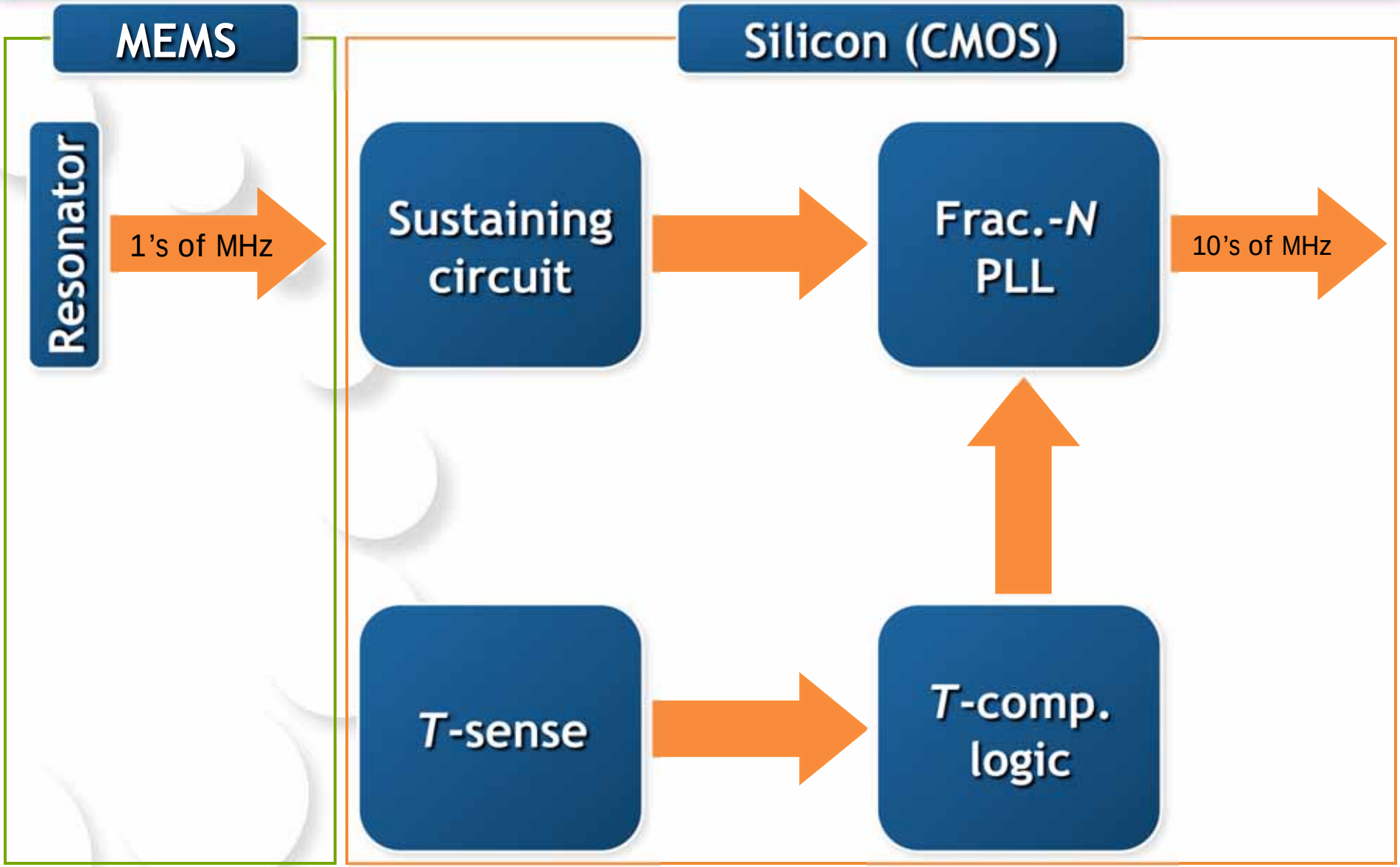


High-Q MHz MEMS resonator



Packaged device

MEMS architecture



MEMS challenges

MEMS-PLL

Resonator

- Requires frequency trimming
- High TC (~20ppm/°C); requires temperature compensation
- Limited power handling; high far-from-carrier phase noise
- Nonlinear transduction; noise upconverts
- High motional impedance; difficult circuit design
- New manufacturing process; added cost
- Hermetic packaging

Architecture

- PLL VCO sets performance
- Loop multiplication is high; noise accumulates
- Fractional-*N* PLL is noisier that integer PLLs
- *T*-comp. induces discrete frequency steps
- High-*Q* benefits of the resonator not realized

Emerging CMOS technologies

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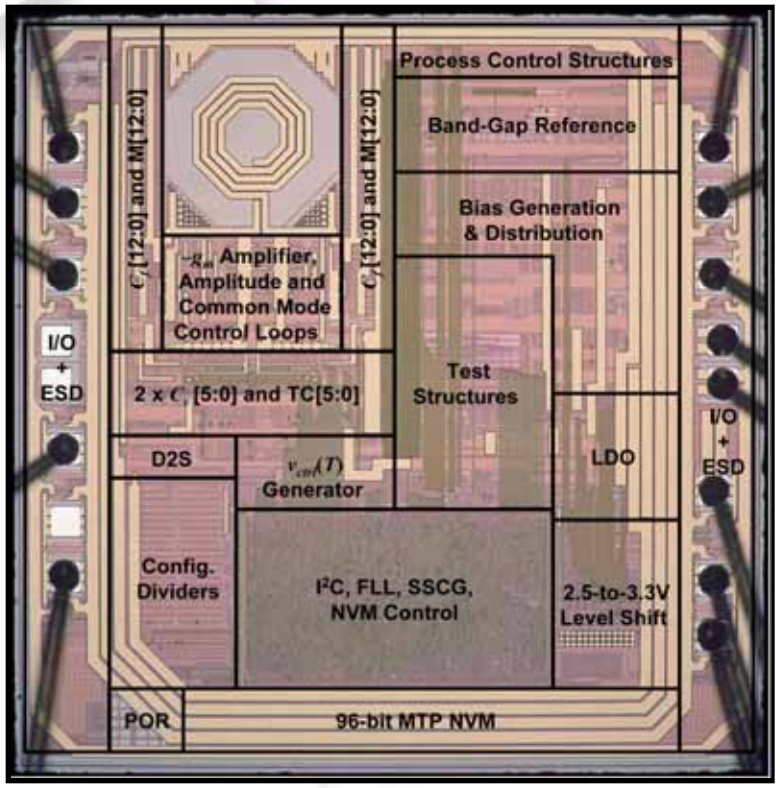
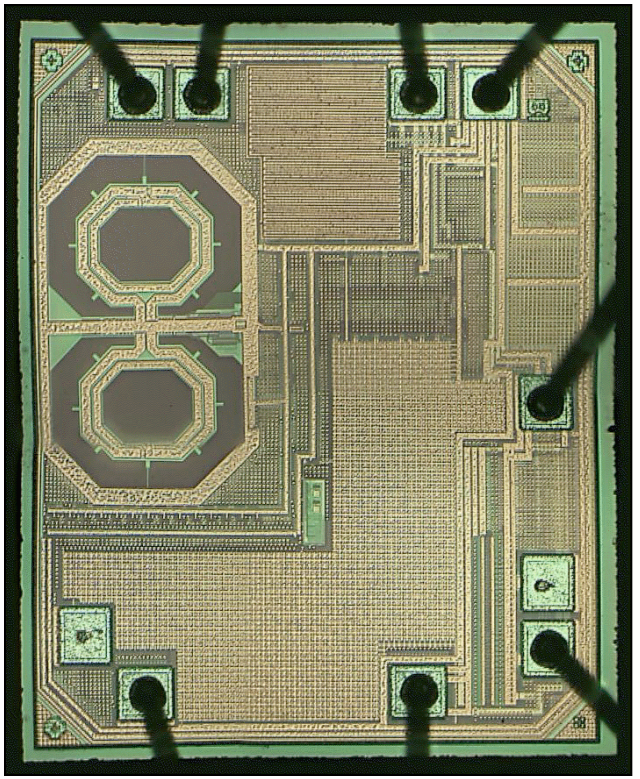


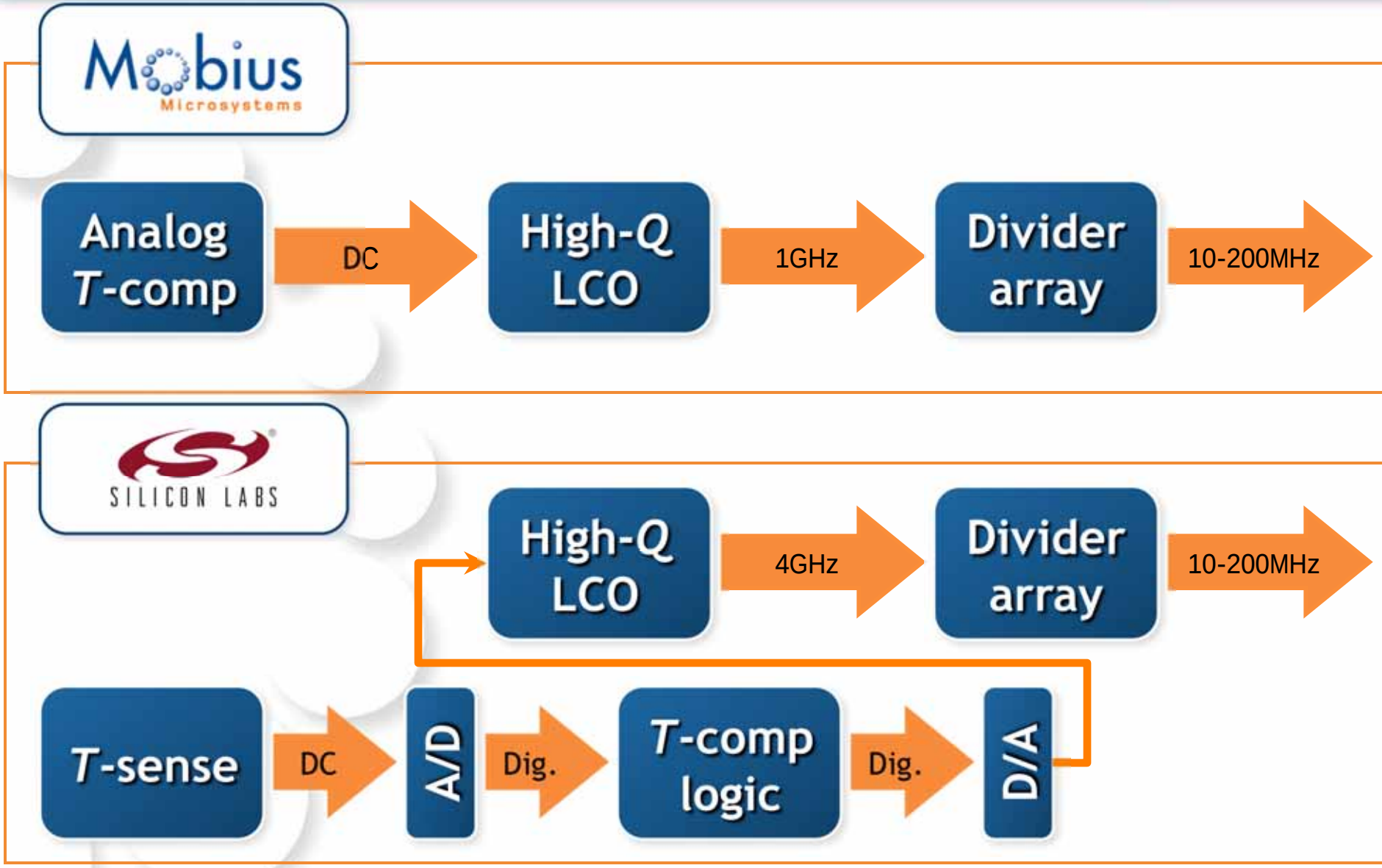
Single-chip, self-referenced CMOS frequency generator (0.25μm)

SILICON LABS



Single-chip, self-referenced CMOS frequency generator (0.13μm)

CMOS oscillator architectures



Conceptual comparison

Möbius Microsystems

	MEMS-PLL	CMOS oscillator
Resonator	• Requires frequency trimming • High TC (~30ppm/°C); material property • Limited power handling • Nonlinear transduction; noise upconv. • High motional impedance • New manufacturing process • Hermetic packaging	• Requires frequency trimming • High TC (~40ppm/°C); multidimensional • Power limited only by technology node • Flicker noise upconversion • Low impedance • Well-established manufacturing platform • Standard packaging
Architecture	• PLL VCO sets noise performance • Loop multiplication is high; noise • Fractional-*N* PLL is noisy • *T*-comp. scheme induces frequency steps • High-*Q* benefits not realized	• *LC* sets noise performance • Frequency division reduces noise • No PLL; free-running • Continuous analog *T*-comp. • Superior performance despite low-*Q* *LC*

SELF-REFERENCED CMOS OSCILLATORS

Section outline

- Motivating concepts
- Architecture
- Implementation challenges
- Implementations
- Production challenges

Motivation and concepts

- Develop an all-silicon frequency source
  - Leverage advances in RF CMOS
  - Explore performance limits of CMOS oscillators
- Conceive an architecture to achieve
  - Low frequency error
  - Low phase noise and low jitter
- Develop with an eye toward wireline timing
  - USB (±500ppm), S-ATA (±350ppm), PCI (±300ppm)
  - But achieving <100ppm would be a great achievement

Motivation and concepts

- Key concepts
  - Far-from-carrier phase noise is the most significant contributor to timing jitter
  - Linear frequency multiplication/division increases/decreases phase noise power quadratically
  - Drift in solid-state oscillators can be understood and compensated
- With these concepts is it possible to develop a monolithic lower-*Q* RF *LC* oscillator and achieve low timing jitter as well as low frequency error?

Motivation and concepts

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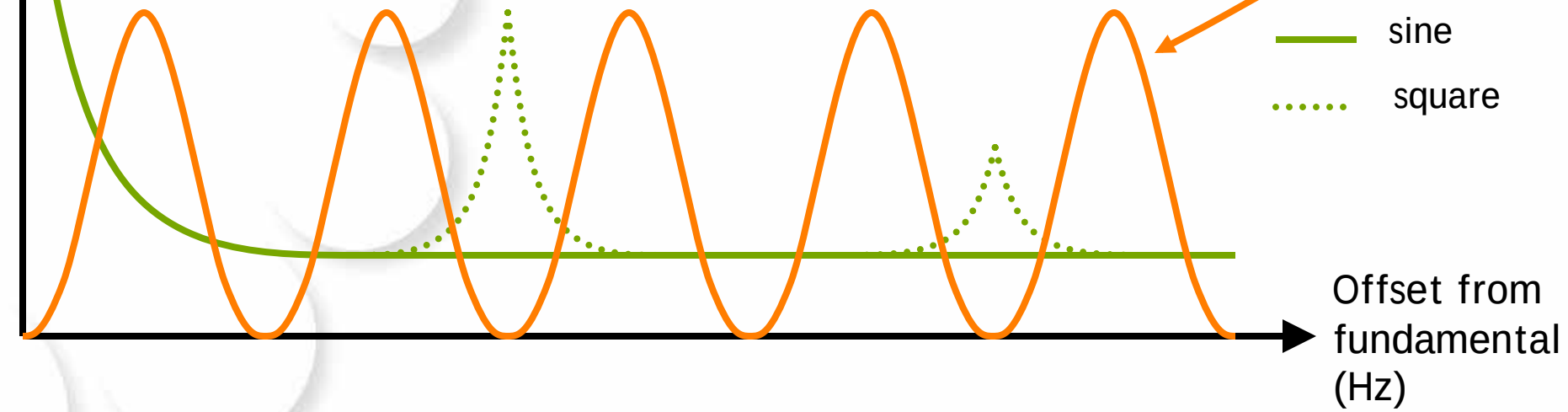
SSB phase noise PSD (dBc/Hz)

$$\sigma_p = \sqrt{\frac{8}{\omega_o^2}\int_0^{\infty}\left(\frac{N_o}{P_o}\right)_{f_m}\sin^2\pi f_m T_o\, df_m}$$

How does phase noise manifest into period jitter?

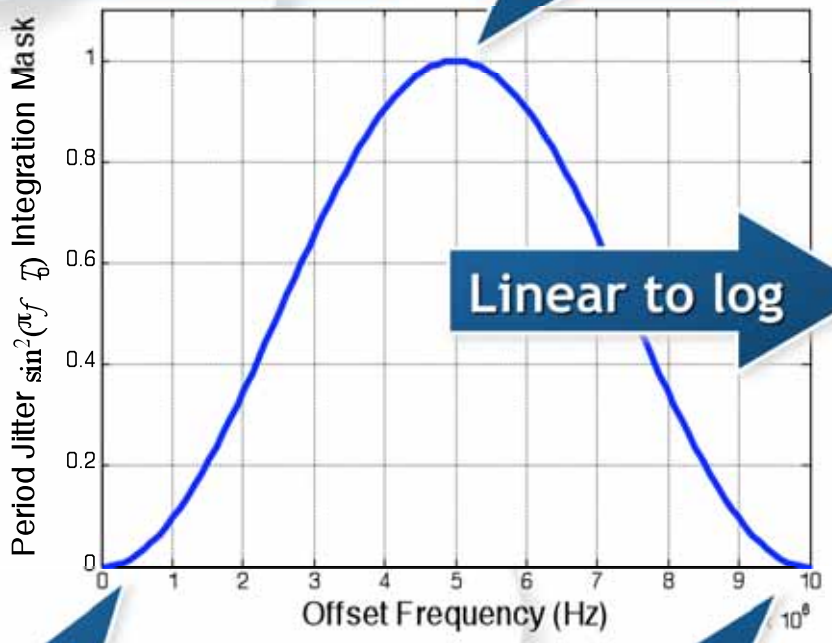
σ_p = RMS period jitter
ω_o = fundamental radian frequency
T_o = fundamental period
f_m = offset frequency from fundamental
$(N_o/P_o)_{fm}$= phase noise at offset f_m from fundamental



Motivation and concepts

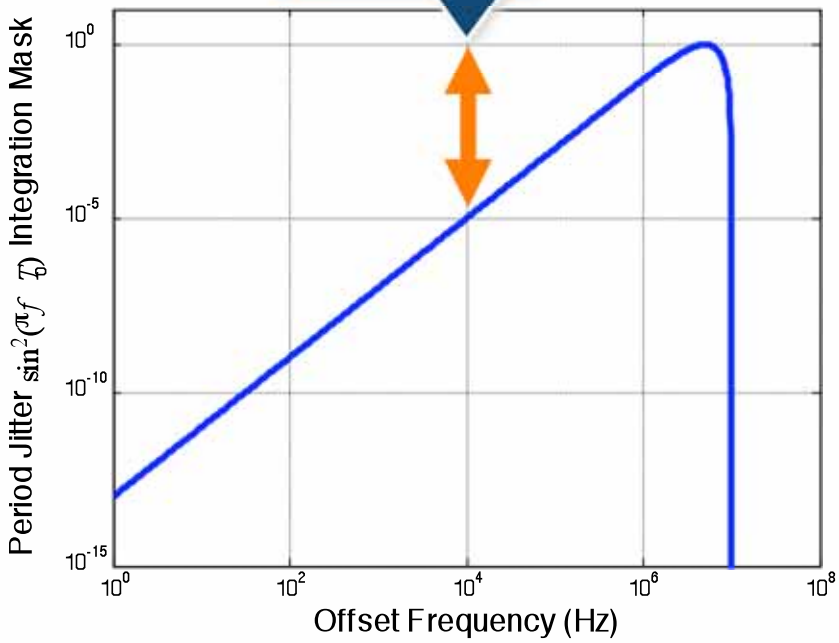
Consider a 10MHz reference

Peak at $f_m = ½ f_o$



Linear to log

-50dB at 10kHz



Null at f_o ($f_m = 0$)

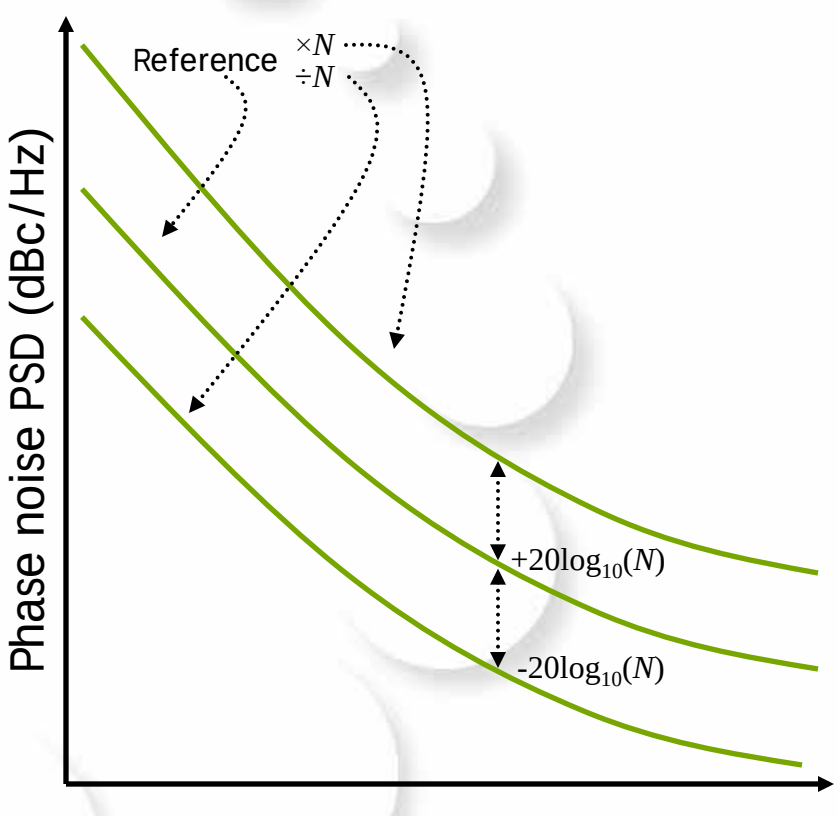
Null at $2f_o$ ($f_m = f_o$)

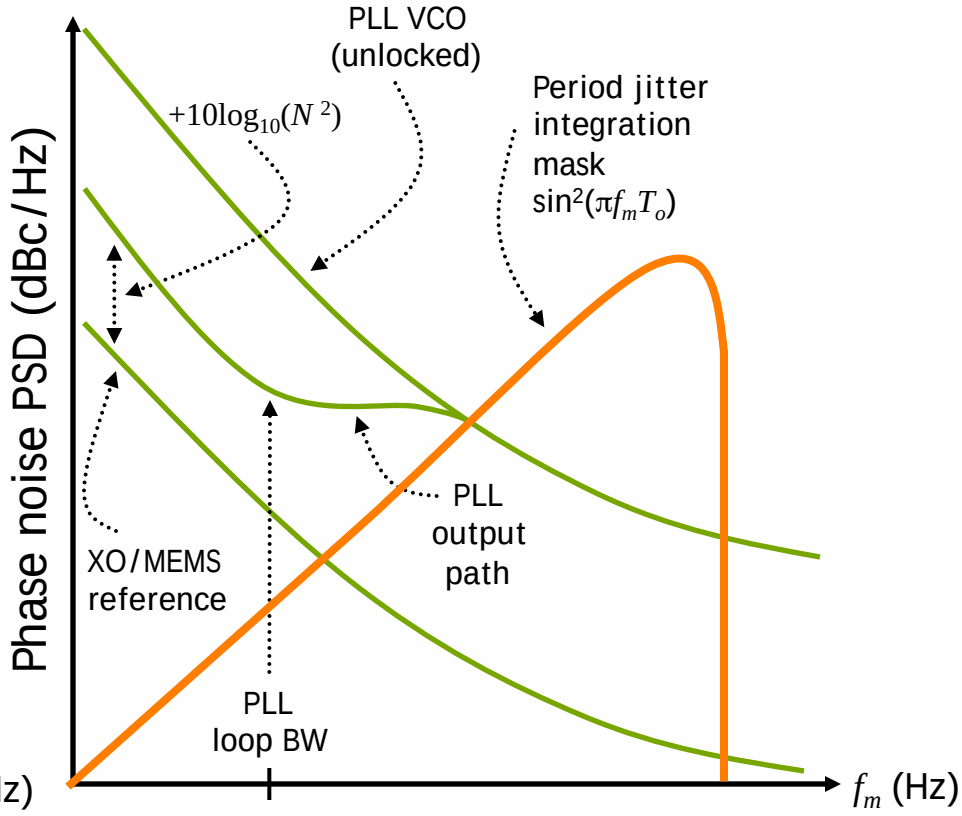
Close-to-carrier phase noise (<10kHz) is attenuated significantly when converting to period jitter

Motivation and concepts

Mobius Microsystems

Close-to-carrier phase noise is attenuated and far-from-carrier phase noise is amplified

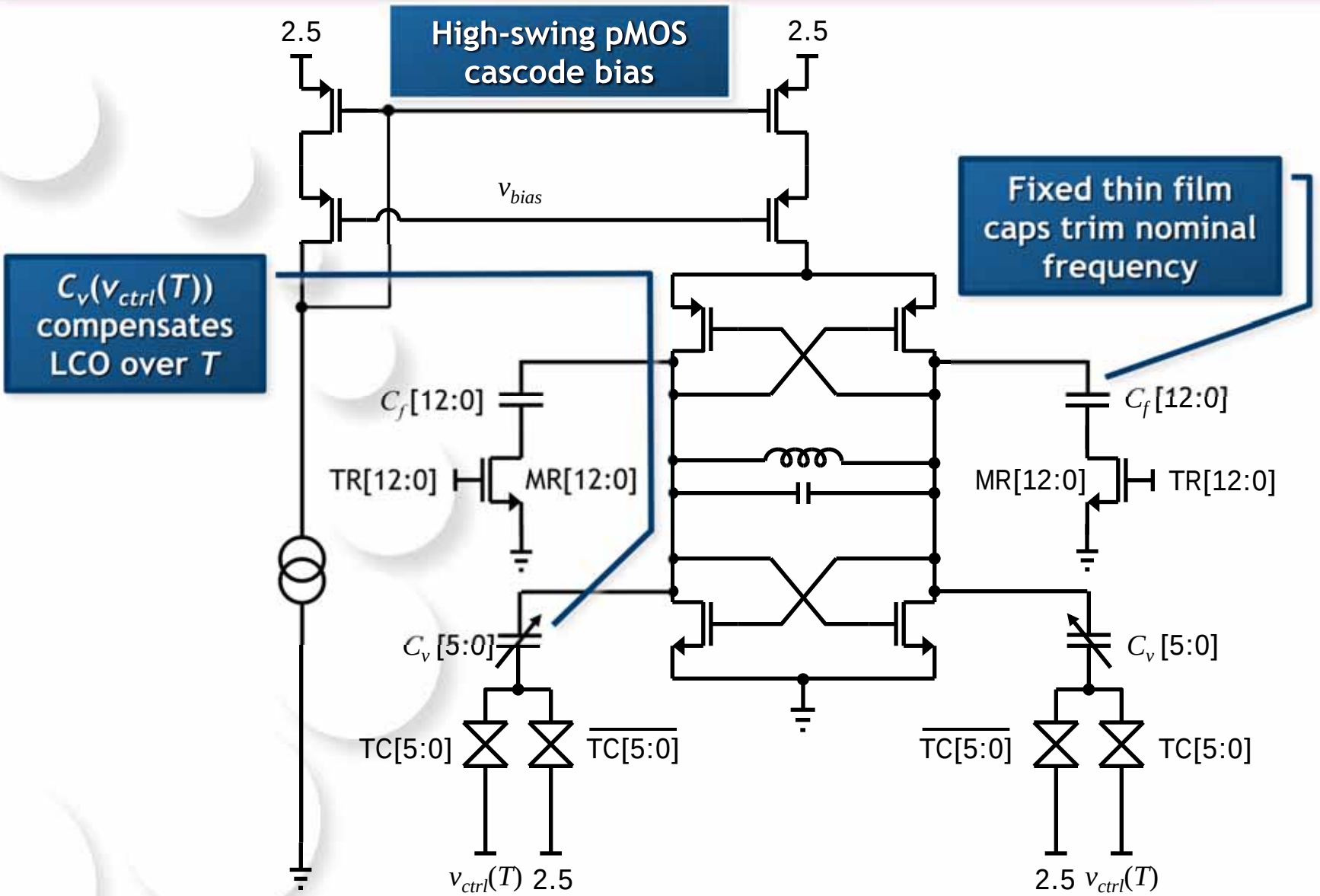




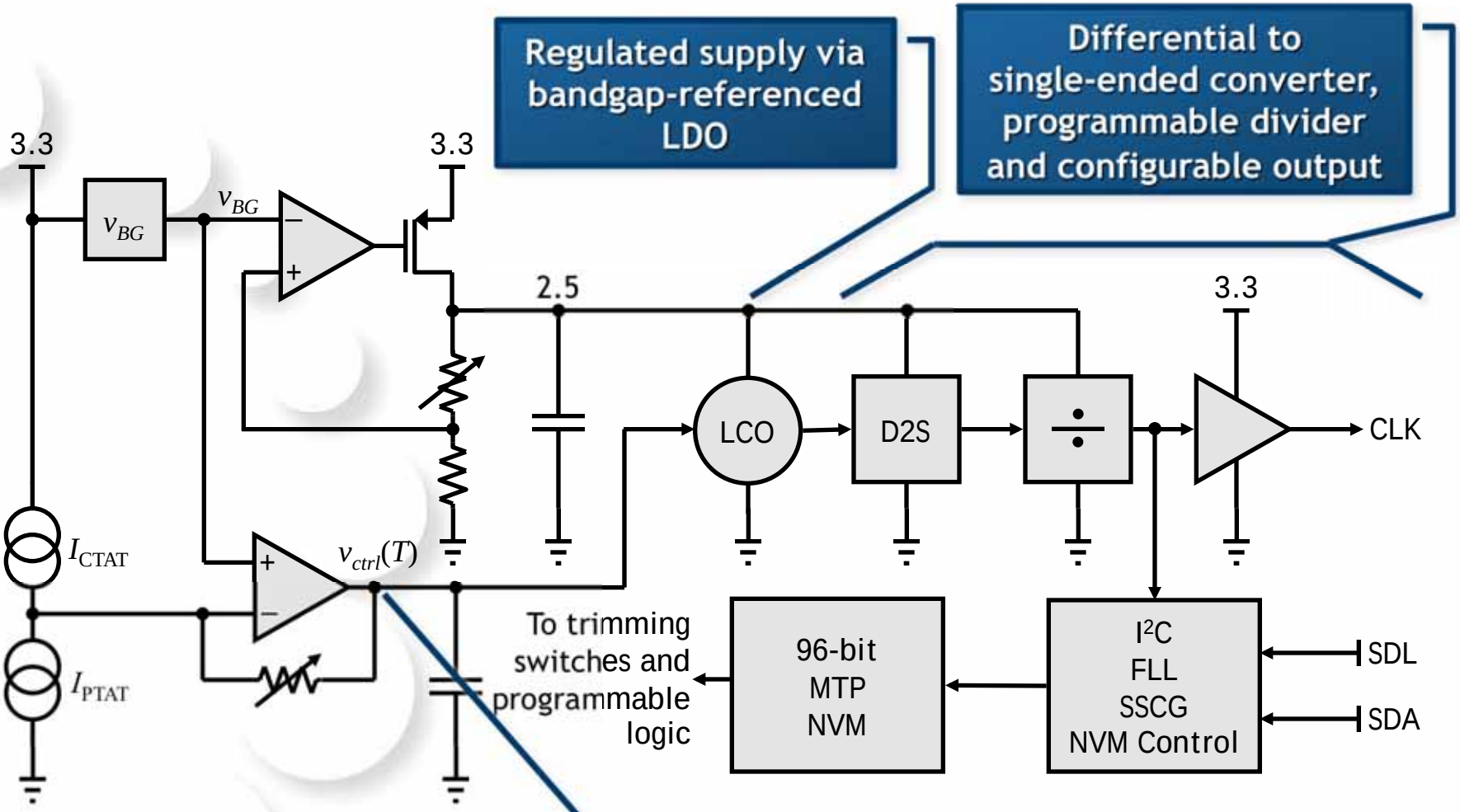
Simplified architecture

- Free-run a CMOS RF *LC* oscillator at over 1GHz
- Design high-resolution process trimming
- Design open-loop temperature compensation
- Actively regulate the power supply
- Frequency divide by a large factor
- Develop a low jitter, stable 10-200MHz reference

Simplified oscillator architecture

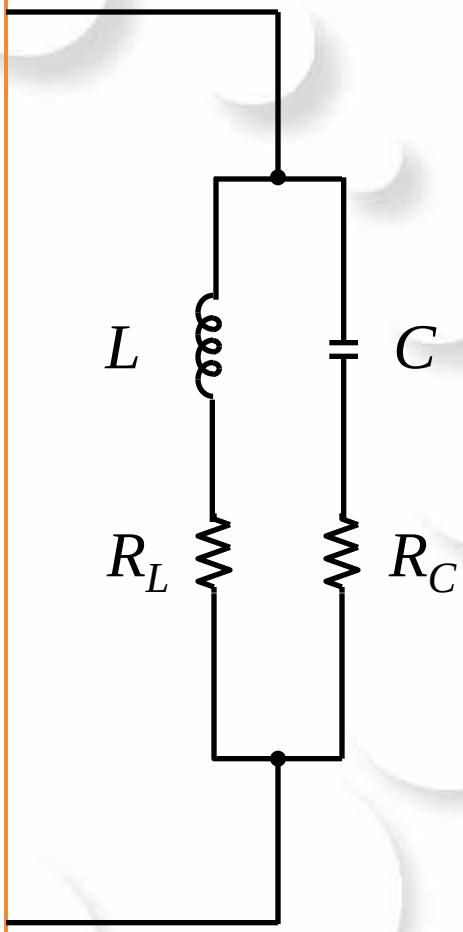


Simplified chip architecture



Implementation challenges

Integrated Tank



1st Order *LC* Dependence

- Due to the parasitic R_L & R_C present in a integrated implementation:

$$\omega \neq \sqrt{1/(LC)}$$

- $R_L(T)$ & $R_C(T)$ cause a temperature-induced frequency drift:

$$\omega_1(T) = \omega_o \sqrt{\frac{CR_L(T)^2 - L}{CR_C(T)^2 - L}} \cong \omega_o \sqrt{1 - \frac{CR_L(T)^2}{L}}$$

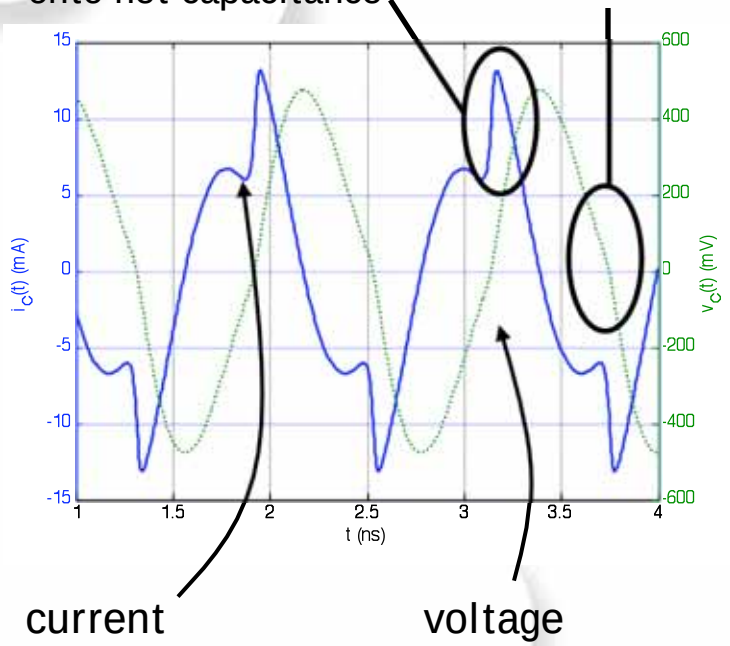
- Temperature drift is negative, concave down and dominated by R_L

Implementation challenges

Harmonic Work Imbalance

g_m-amp injects current onto net capacitance

Waveform is distorted

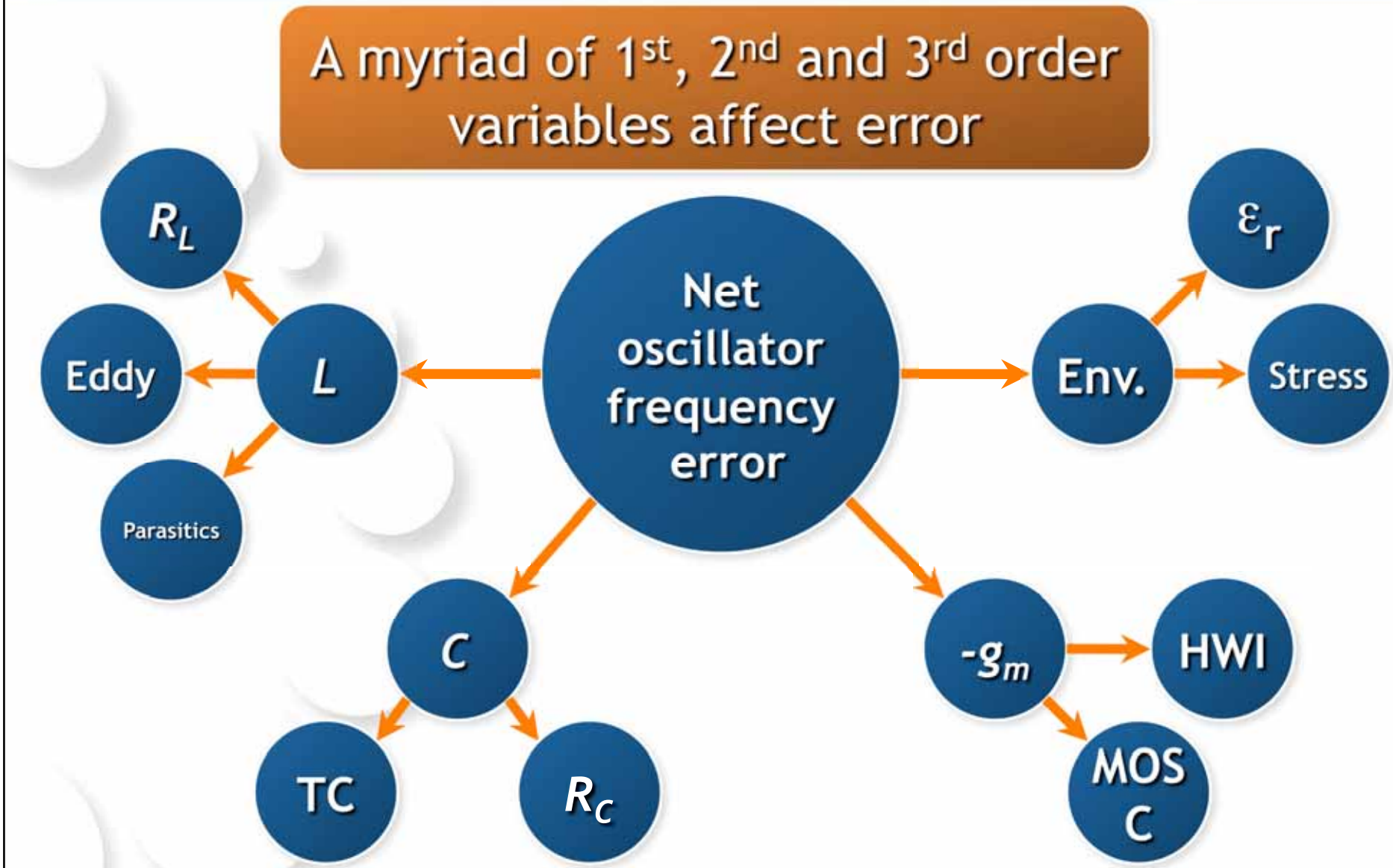


$$\omega_o = \omega_1\left(1 - \frac{1}{2Q^2}\sum_{n=2}^{\infty}\frac{n^2}{n^2-1}h_{i(n)}^2\right)$$

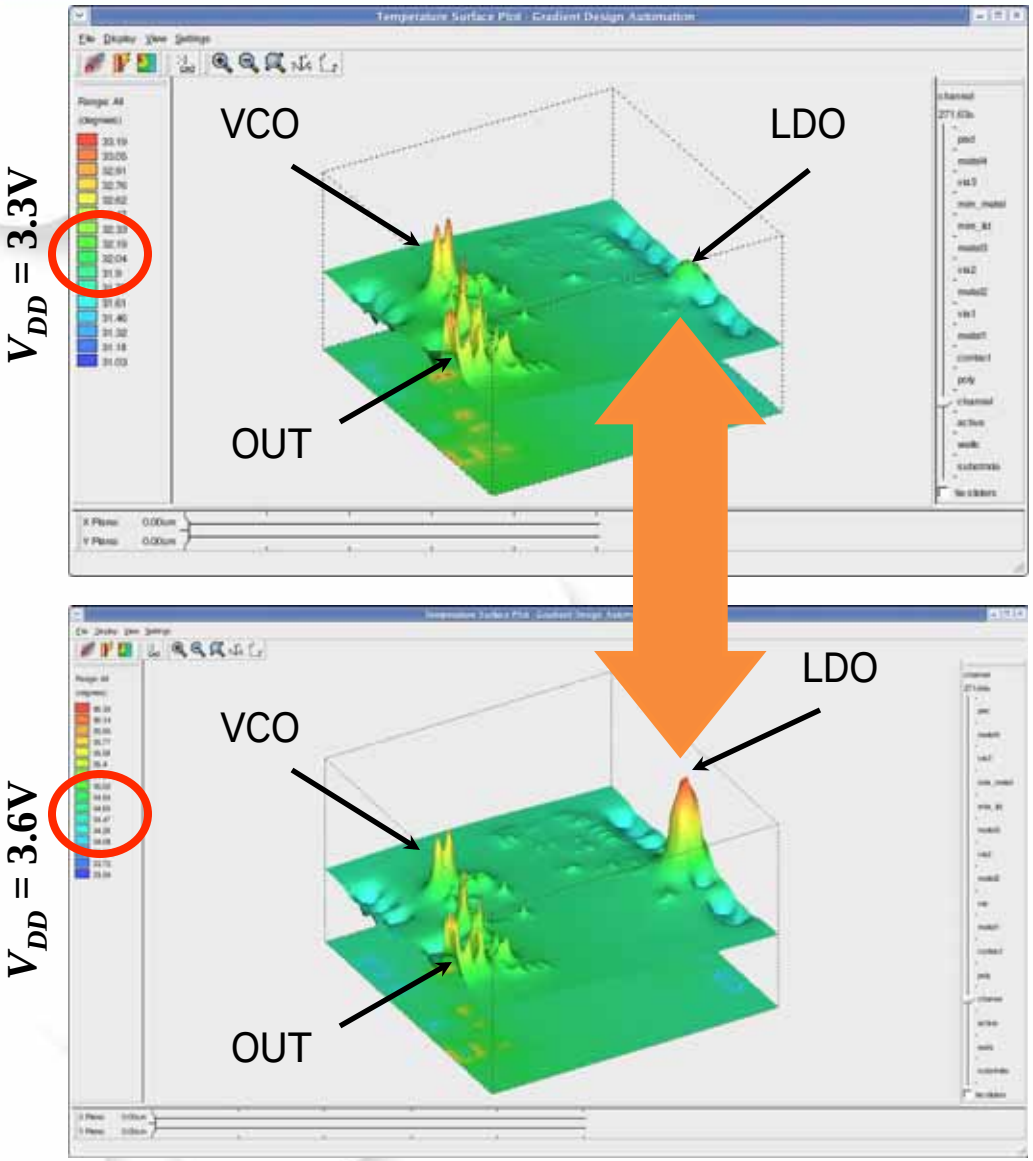
Bias Dependence

- The transconductor causes a harmonic work imbalance (HWI) between *C* and *L* which leads to drift
- Frequency drift due to harmonic work imbalance is a function of the normalized Fourier coefficients, $h_i(n)$, of the current waveform
- Note, as $Q \rightarrow \infty$, drift due to harmonic work imbalance approaches 0

Implementation challenges



Implementation challenges



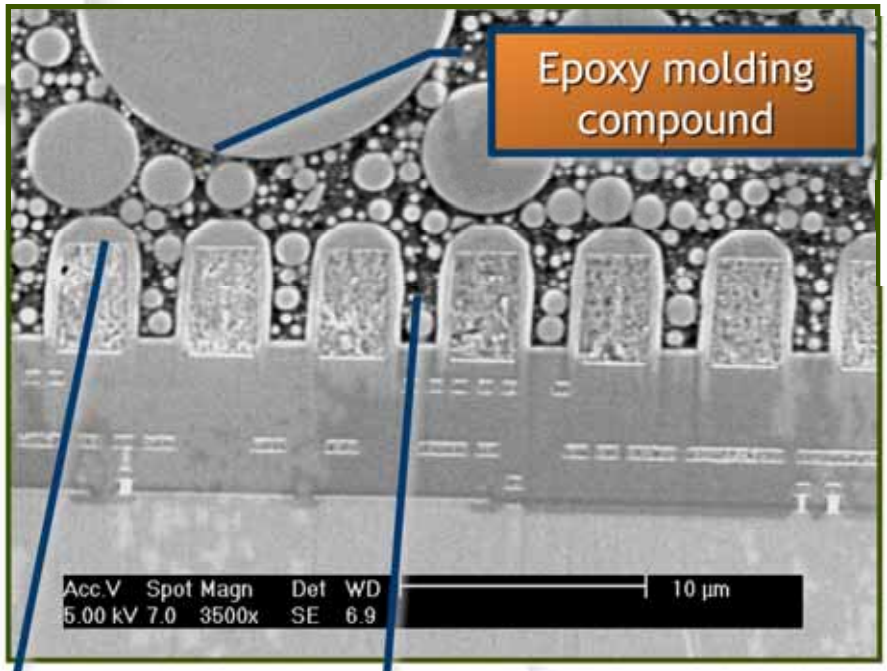
Thermal Sensitivity

- *T*-comp. circuits are highly sensitive to self-heating effects in packages with high Θ_{JA}
- Locally, temperature can increase by ~3°C
- Globally, such increases raise the net die temperature by 2°C
- These mismatches introduce freq. error

Implementation challenges

Mobius Microsystems

Plastic Encapsulation



Environmental Sensitivities

- Molding compound shifts frequency due to fringing *E*-field (new ε_r)
- Molding compound can impart mechanical stress on last metal interconnect
- Both are can be contained, but illustrate additional implementation challenges
- Planar last metal processes are less sensitive

Production challenges

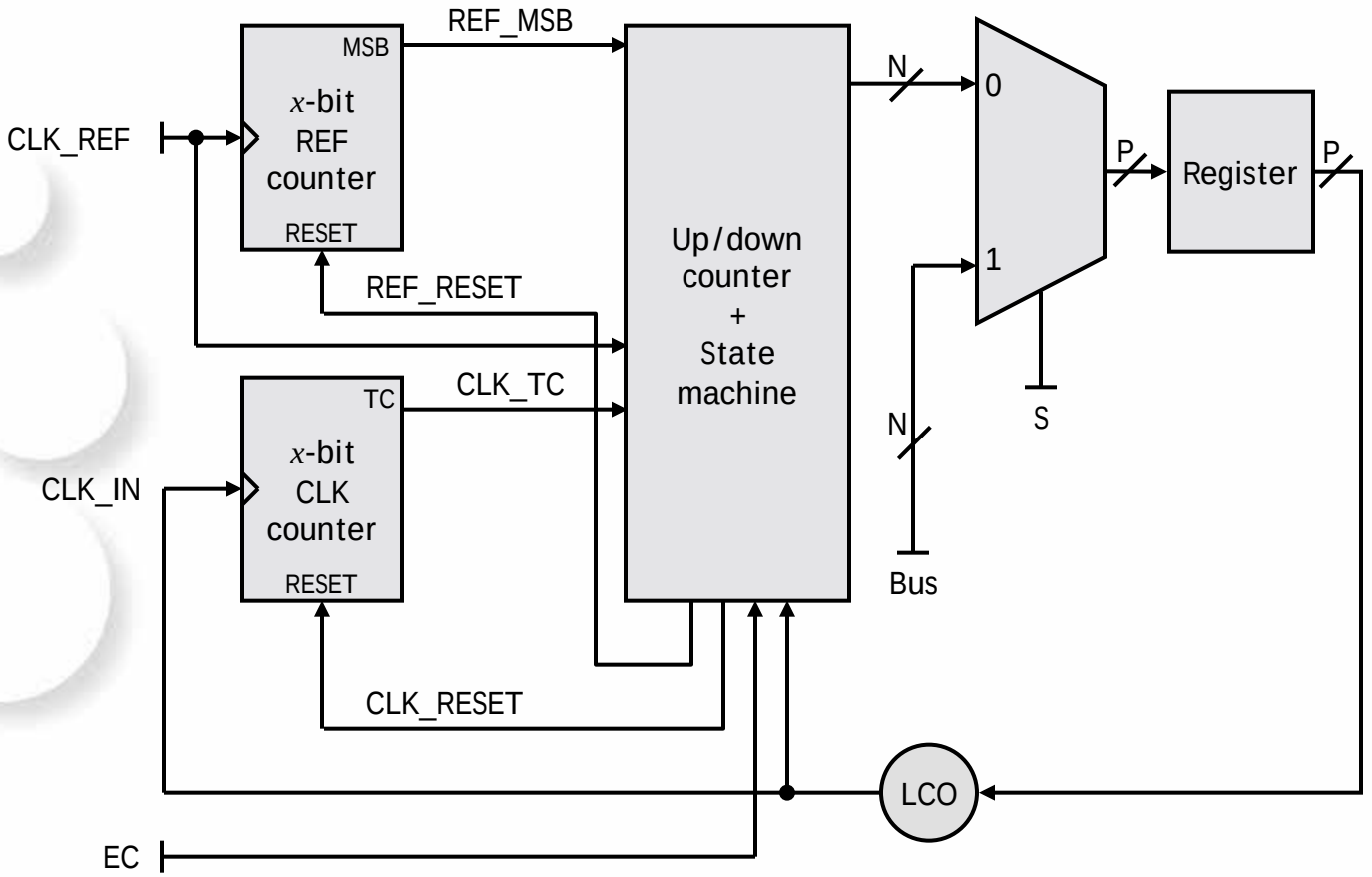
- Each design effort is a major challenge
  - Models are typically missing TC parameters
  - 2nd and 3rd order effects do not sim. accurately
- Yet, with the presented architecture:
  - any device can be trimmed ideally,
  - but can each be trimmed economically?
- Process variation causes:
  - The frequency to vary from part to part
  - The TC to vary from part to part (this is why the two are orthogonal in *Mobius*' architecture)

Production challenges

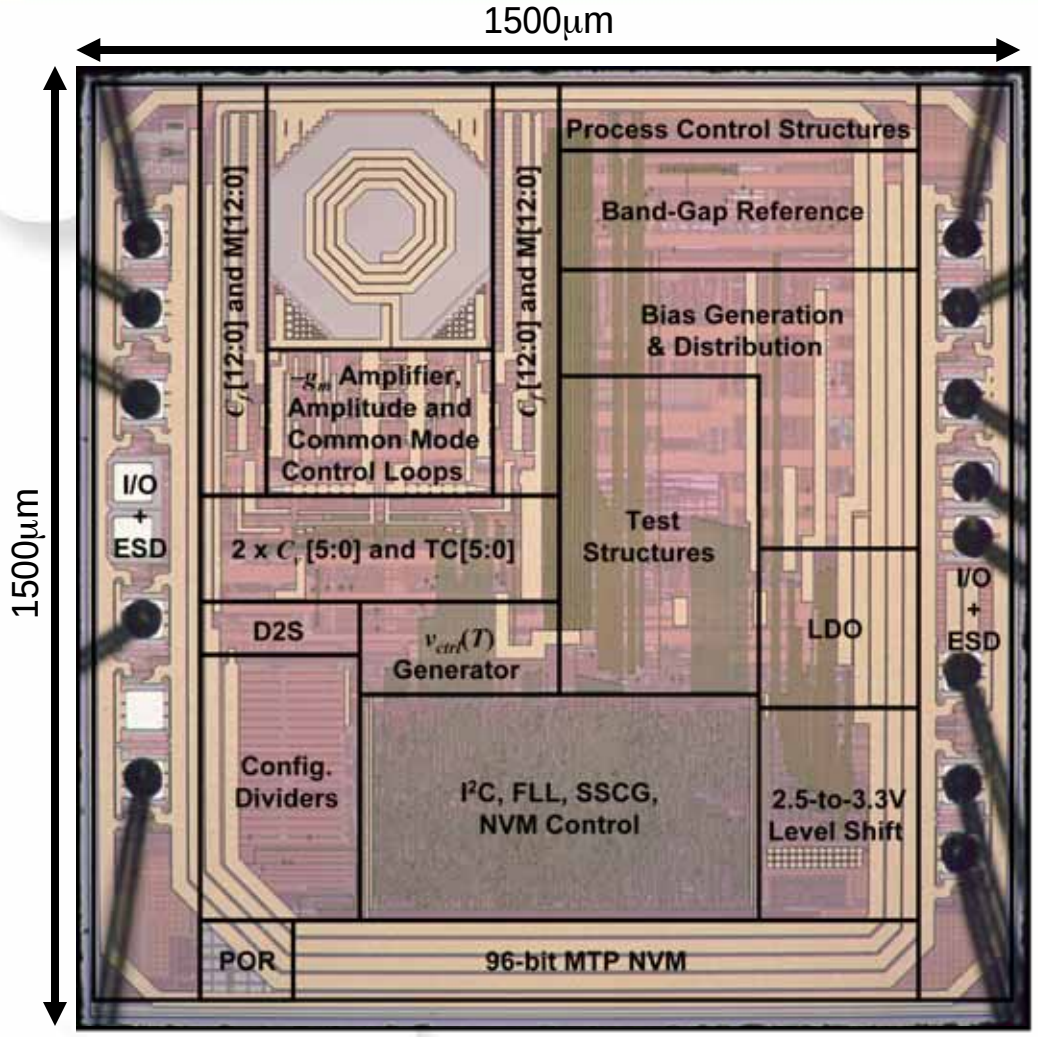
Mobius Microsystems

To trim the nominal frequency a digital FLL runs counting "races" between a precision reference and the LCO

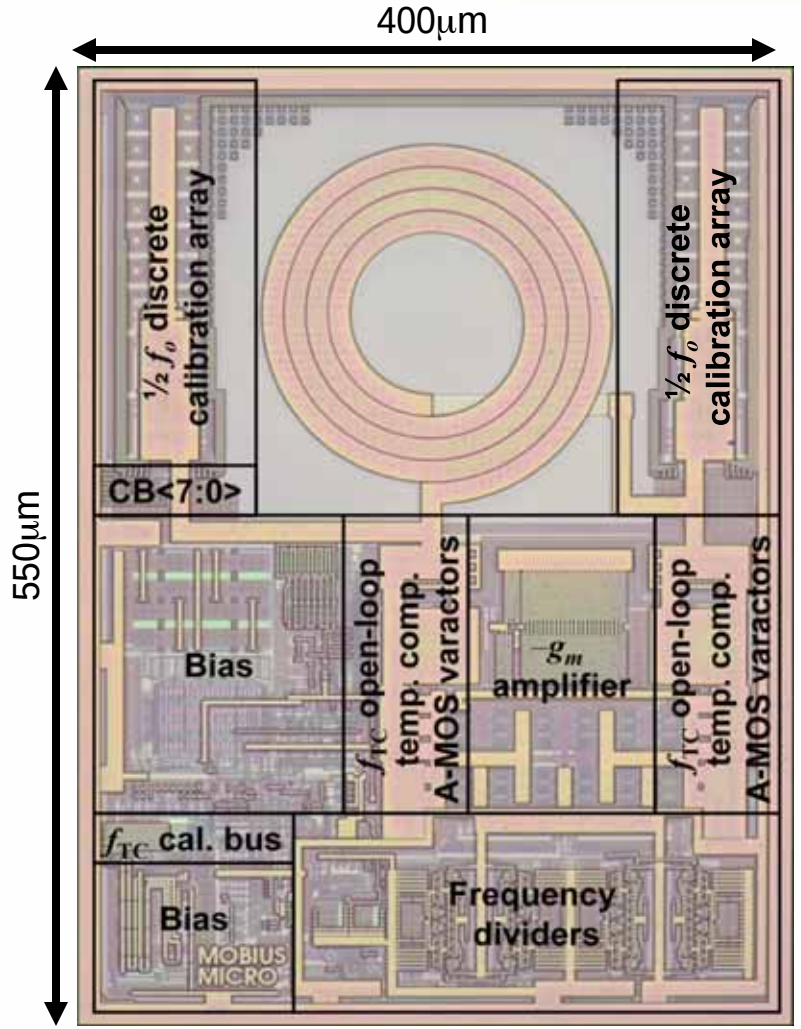
A similar and propriety technique is used to trim the TC for each device



Recently published implementations



Michael S. McCorquodale, *et al.*, "A 0.5–480MHz Self-Referenced CMOS Clock Generator with 90ppm Total Frequency Error and Spread Spectrum Capability," *IEEE Int. Solid State Circuits Conf. Dig. of Tech. Papers*, San Francisco, CA 2008.



Michael S. McCorquodale, *et al.*, "A Monolithic and Self-Referenced RF LC Clock Generator Compliant with USB 2.0," *IEEE J. of Solid State Circuits*, vol. 42, no. 2, Feb. 2007, pp. 385-399.

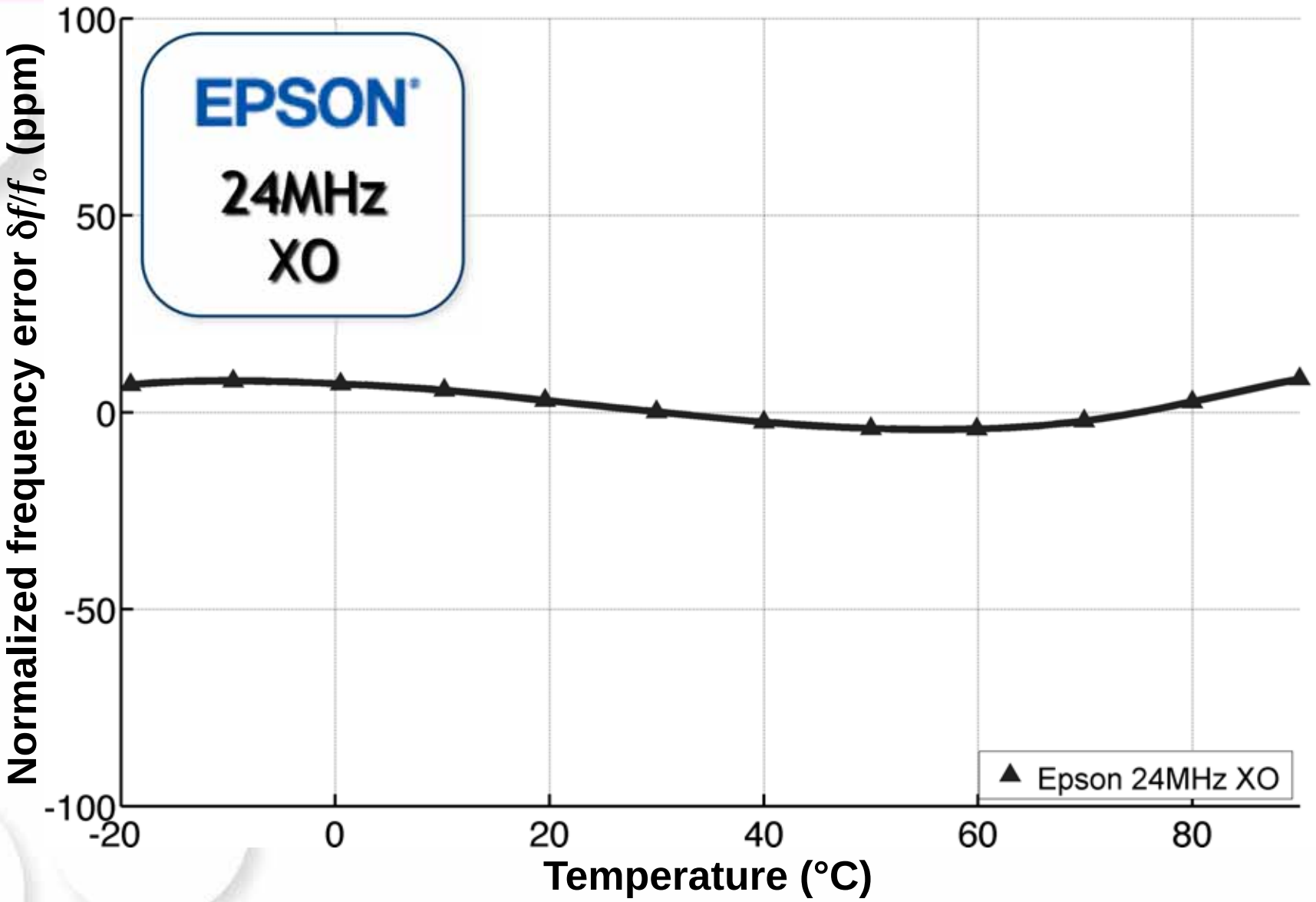
PERFORMANCE BENCHMARKING

Section outline

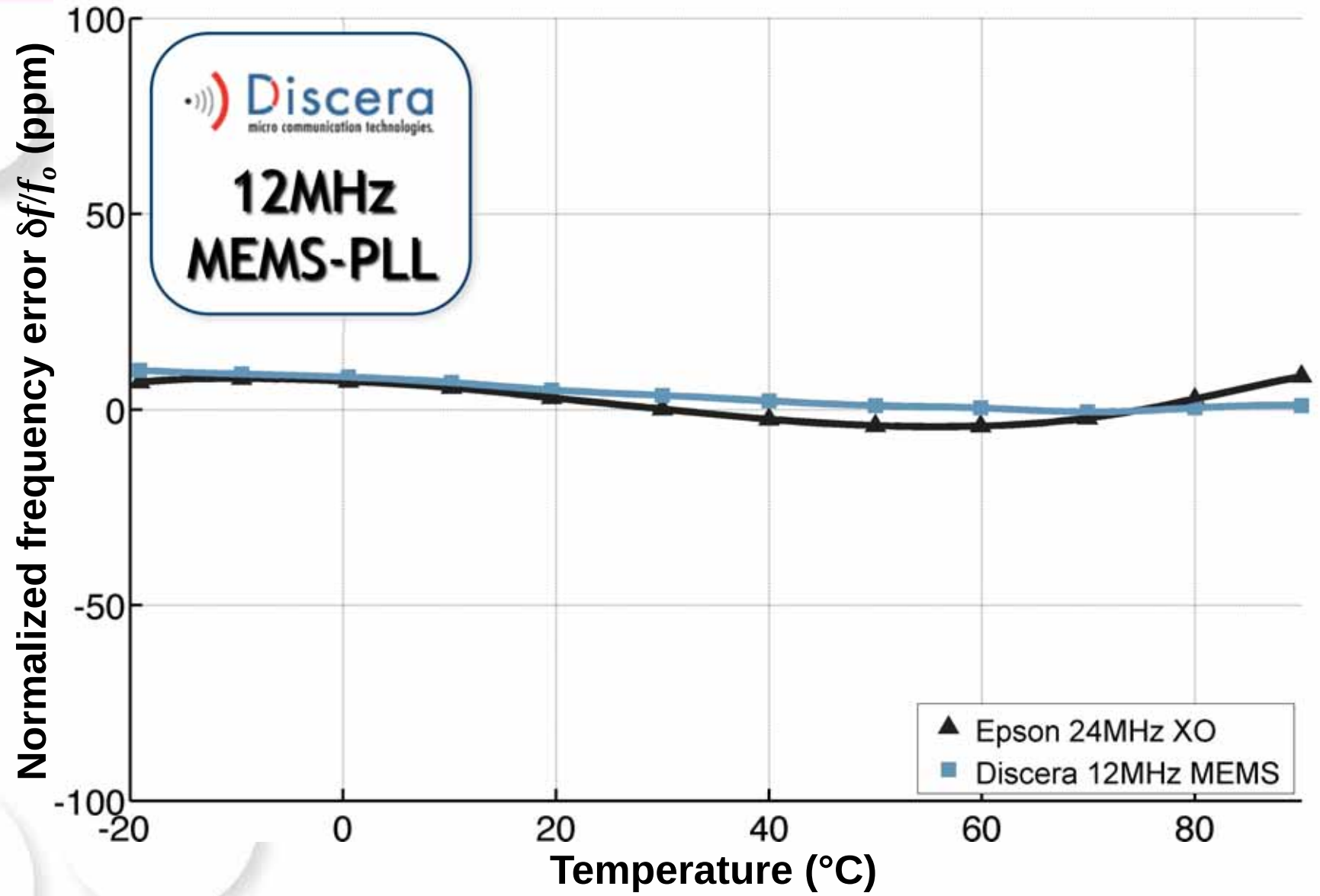
- Frequency generators
  - *Epson* 24MHz XO
  - *Discera*/*SiTime* 12/20MHz MEMS-referenced PLLs
  - *SiLabs*/**Mobius* 24MHz CMOS oscillators
- Measure
  - Total frequency error from -20C to 90°C
  - Single sideband phase noise PSD
  - RMS phase jitter integrated from 12kHz to 5MHz
  - RMS period and cycle-to-cycle jitter
  - Start-up latency
  - Power dissipation

*Performance data reported on Mobius' product herein is for its 2nd generation device; performance has not been published academically though the datasheet is published and the reported product is currently sampling

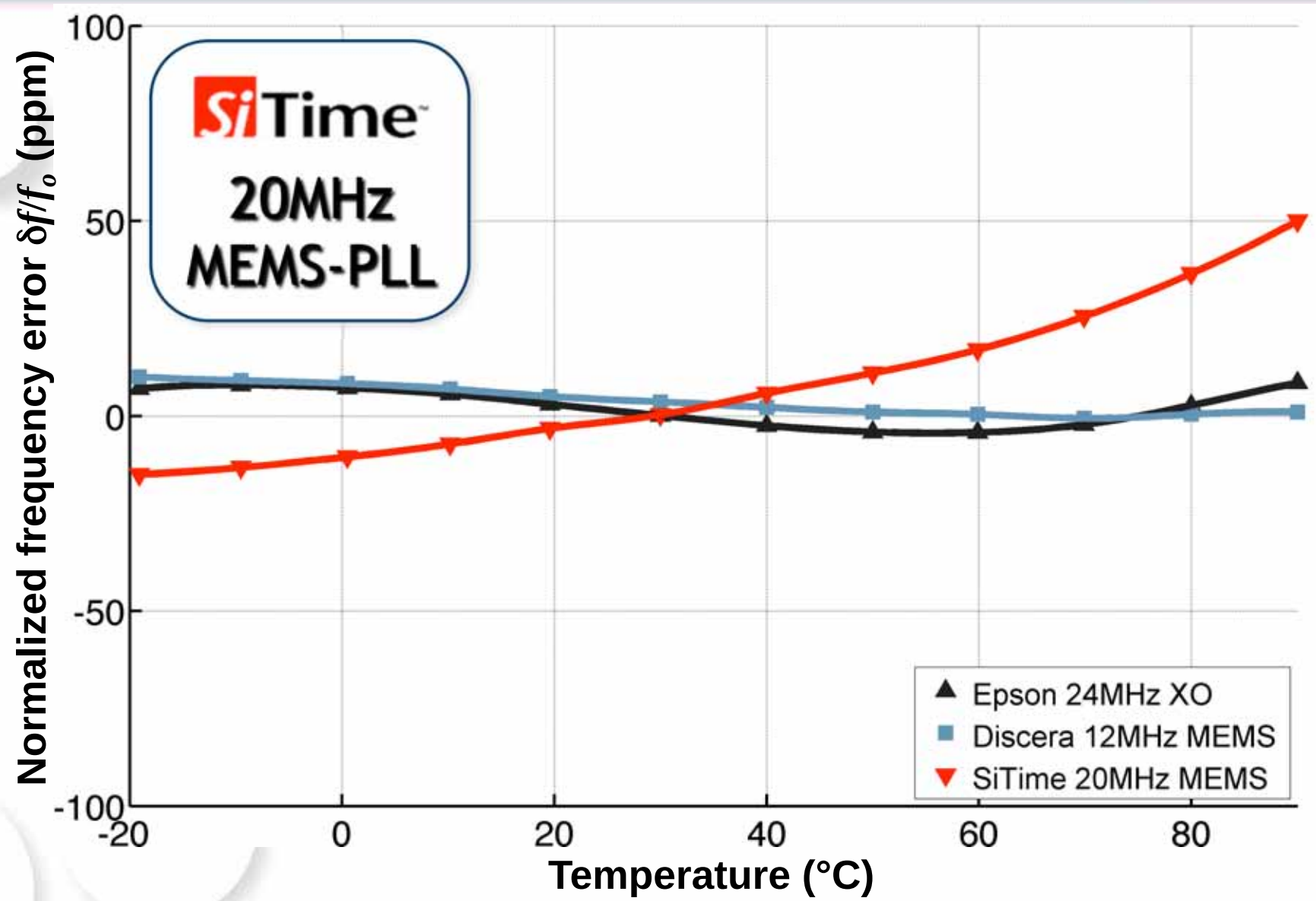
Total frequency error



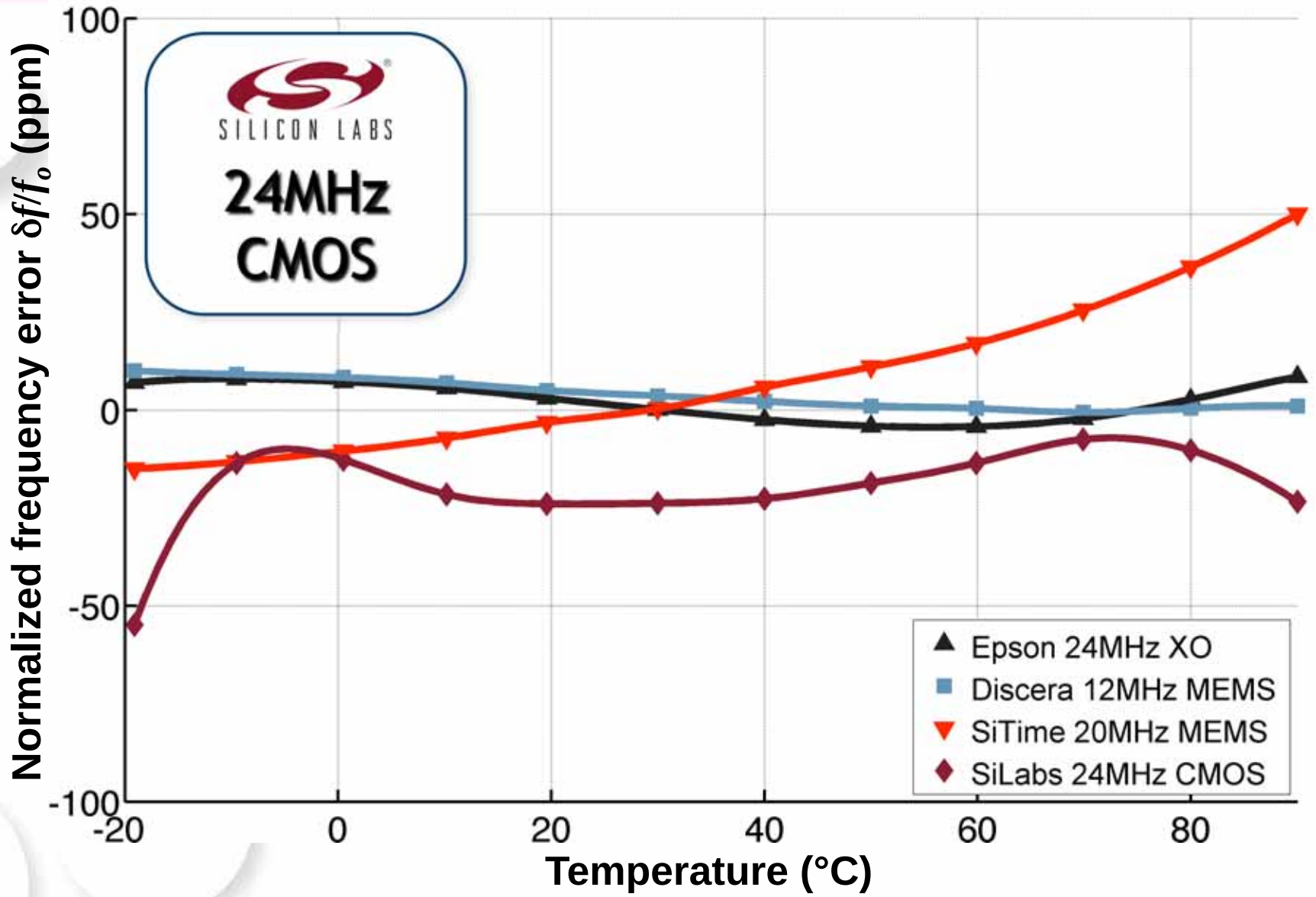
Total frequency error



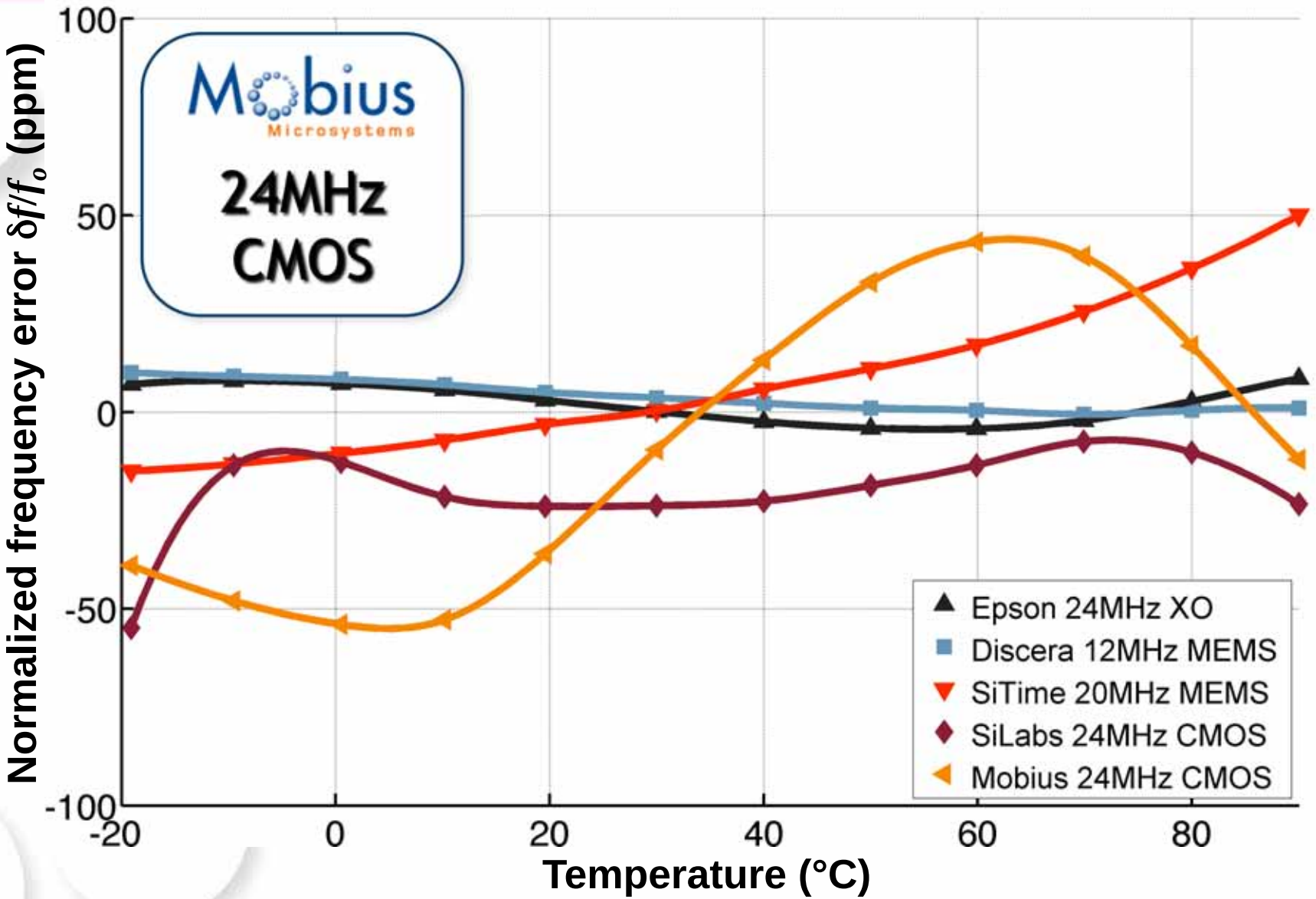
Total frequency error



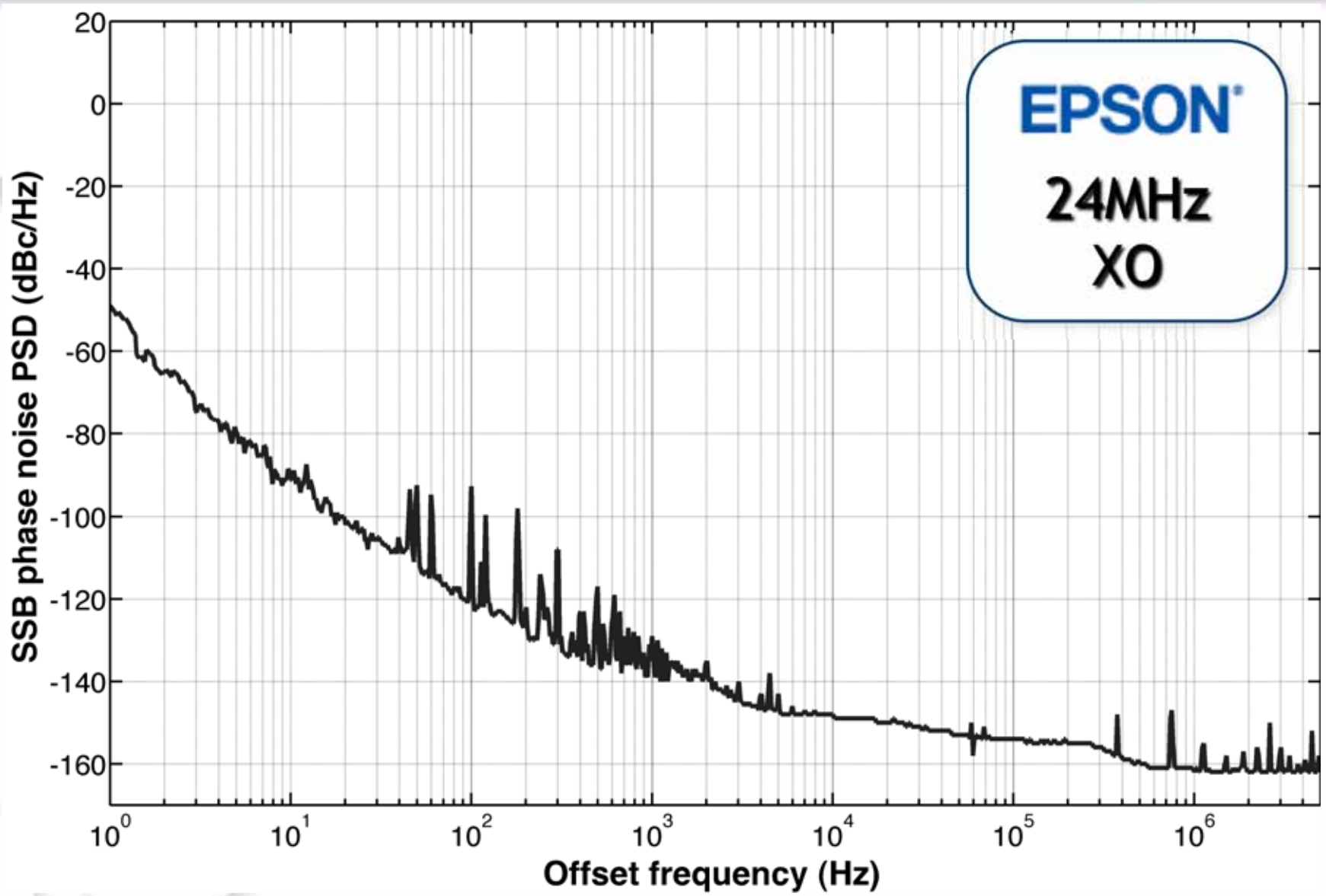
Total frequency error



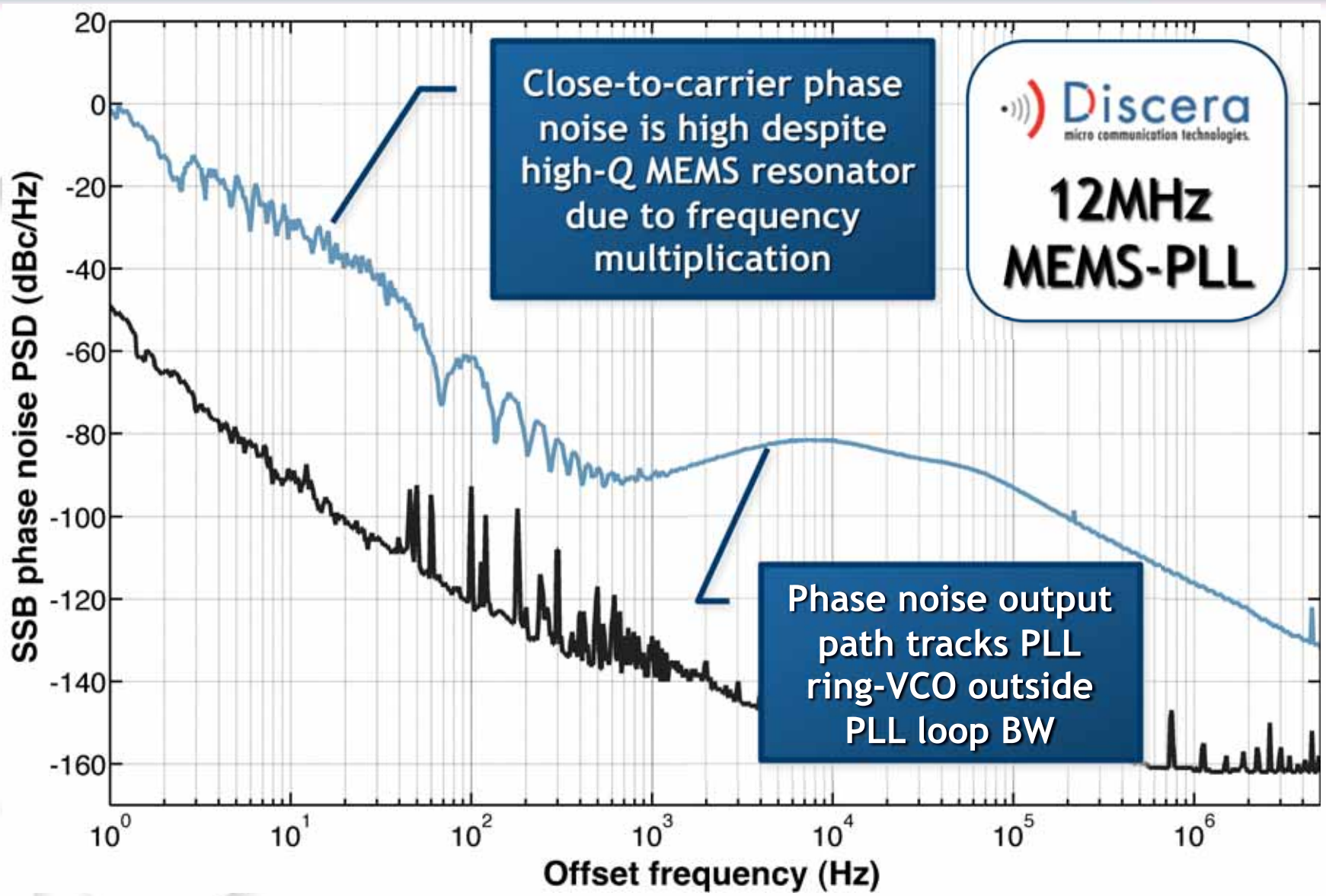
Total frequency error



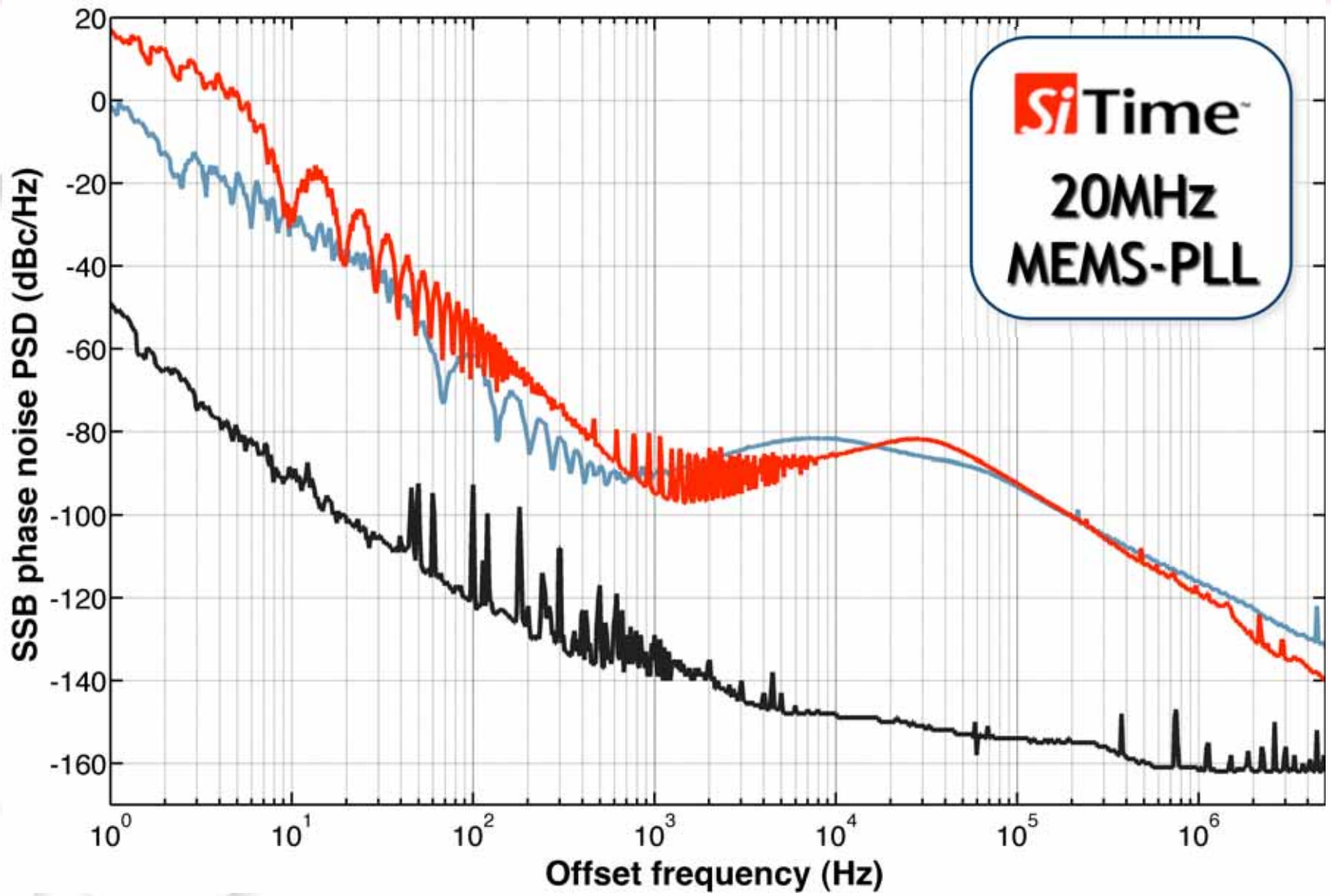
SSB phase noise PSD



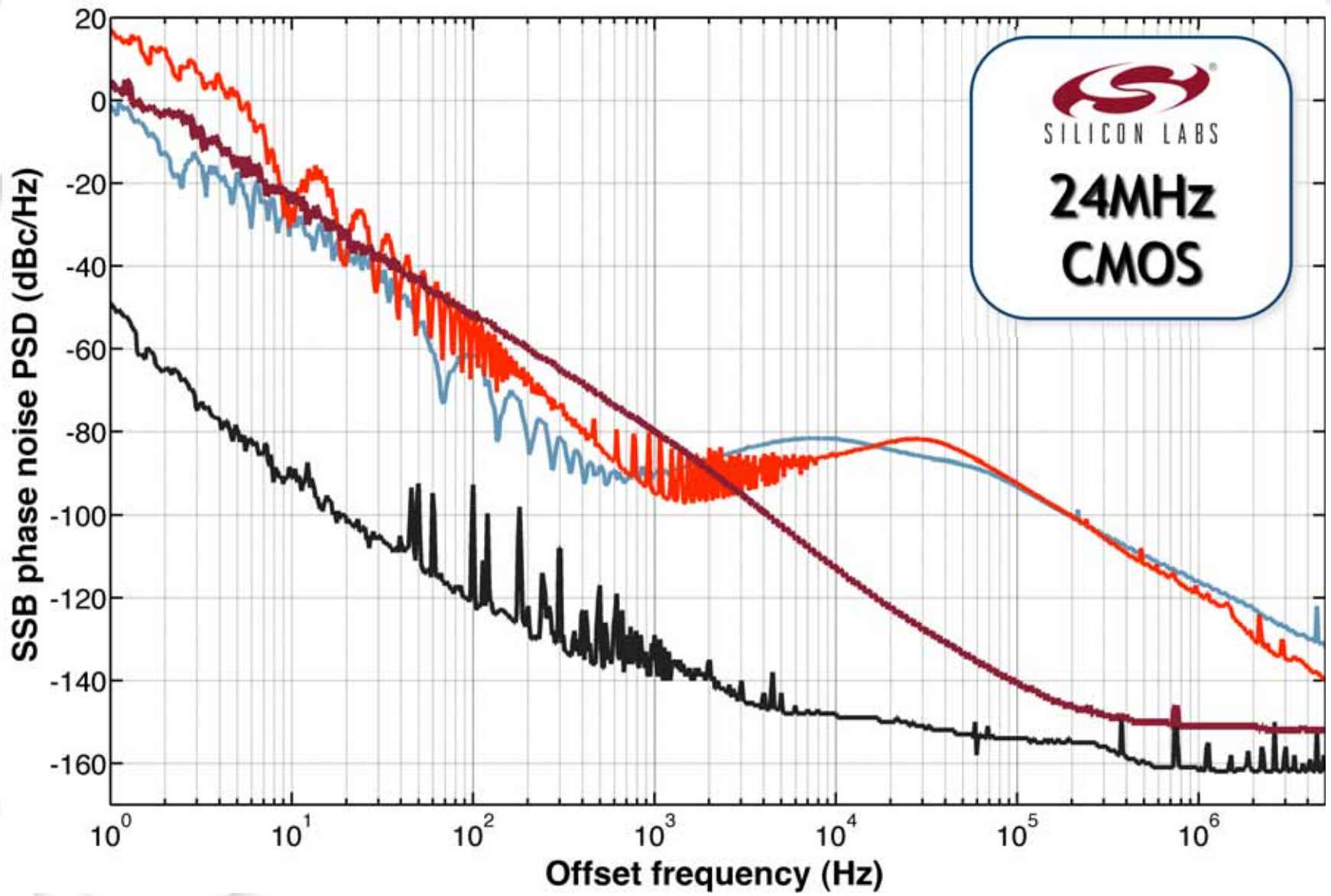
SSB phase noise PSD



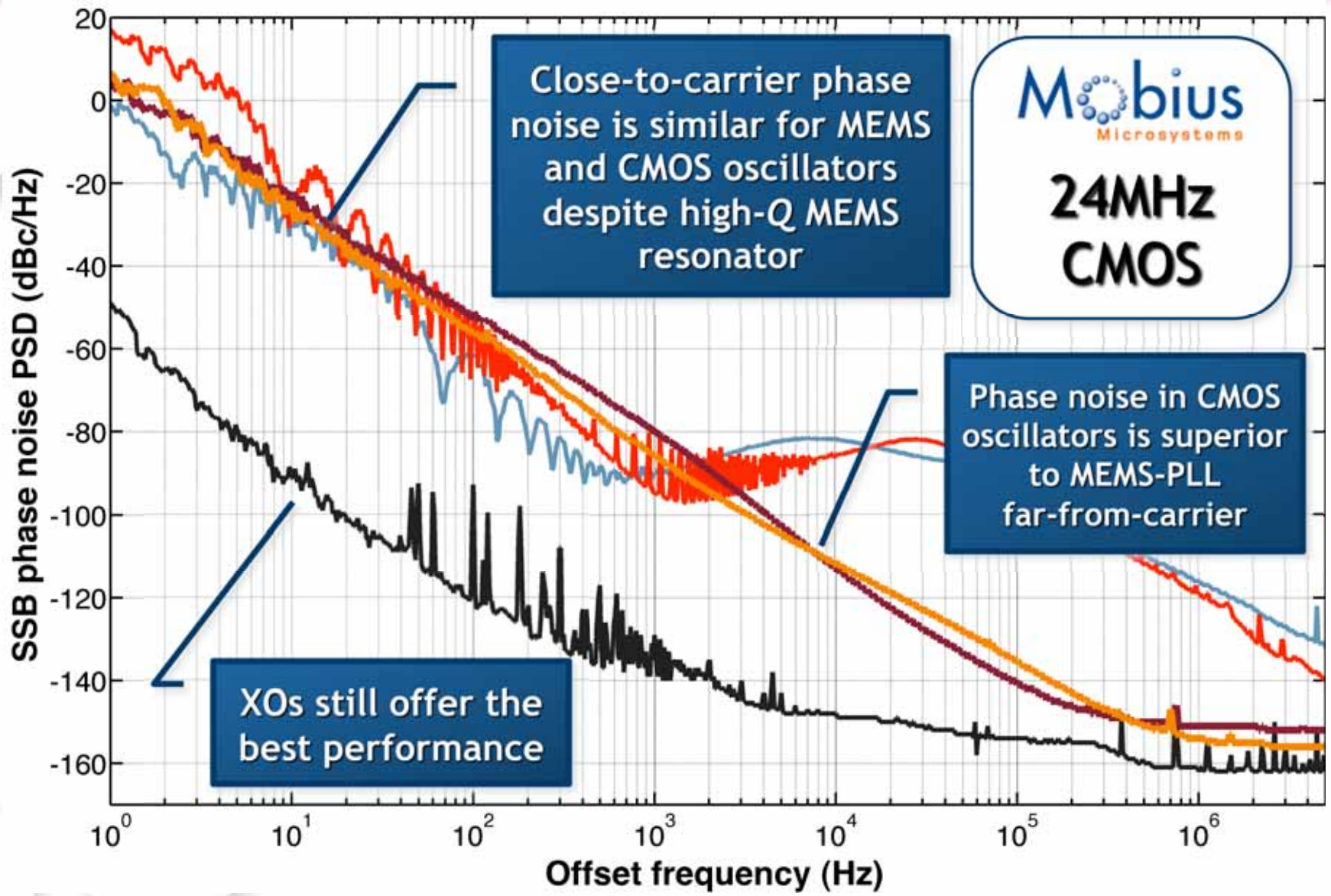
SSB phase noise PSD



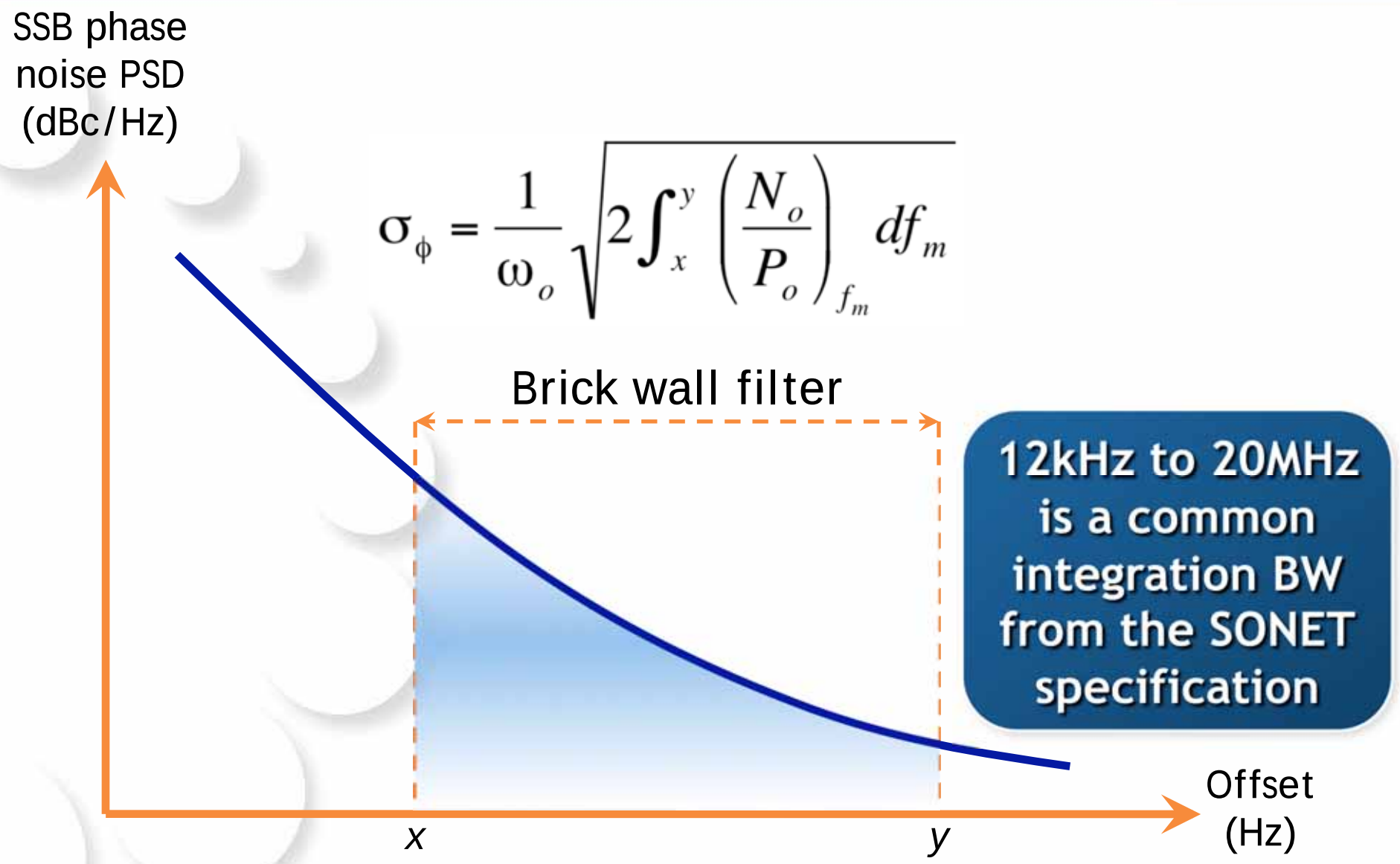
SSB phase noise PSD



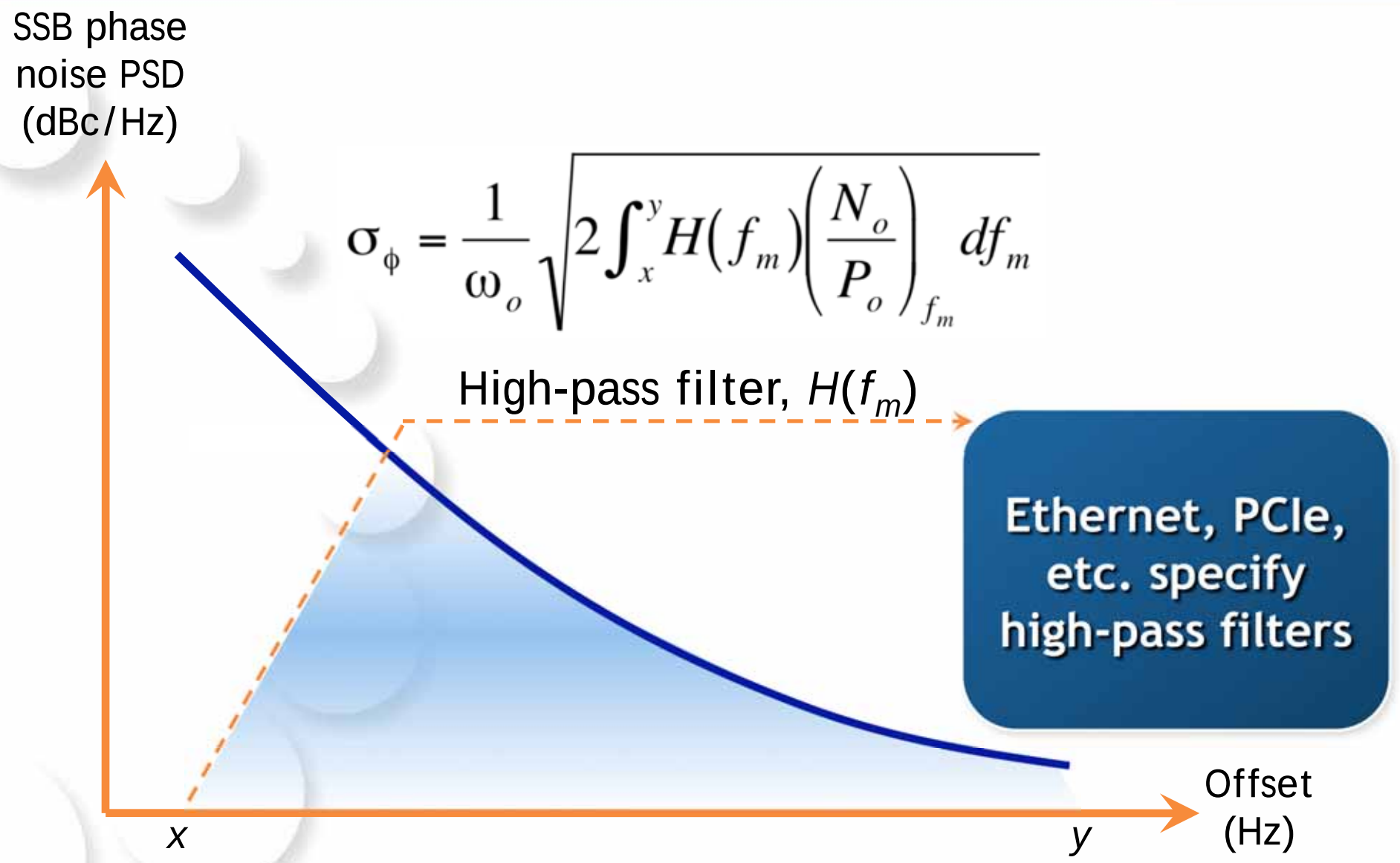
SSB phase noise PSD



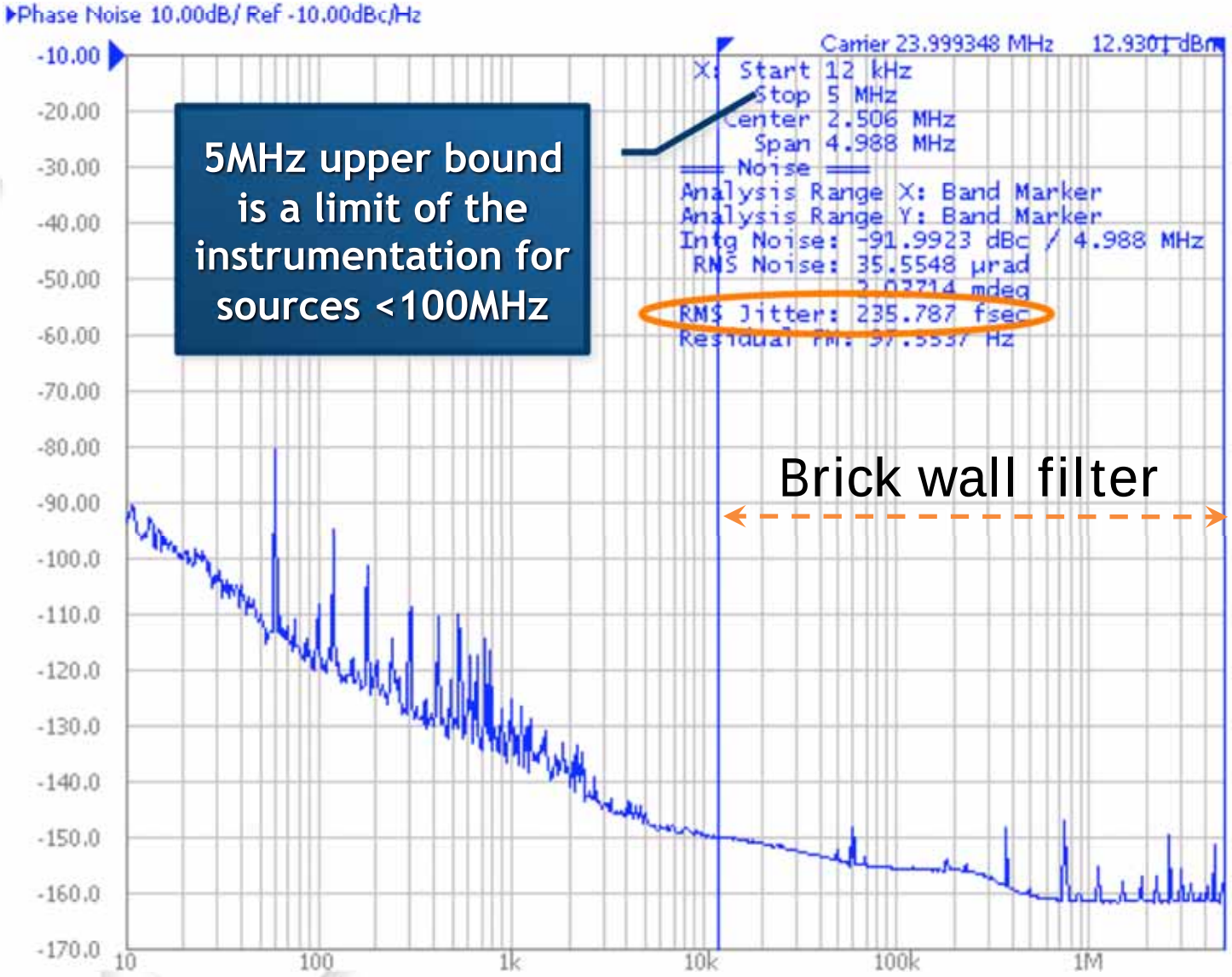
Integrated phase jitter



Integrated phase jitter



RMS phase jitter (12kHz to 5MHz)



5MHz upper bound is a limit of the instrumentation for sources <100MHz

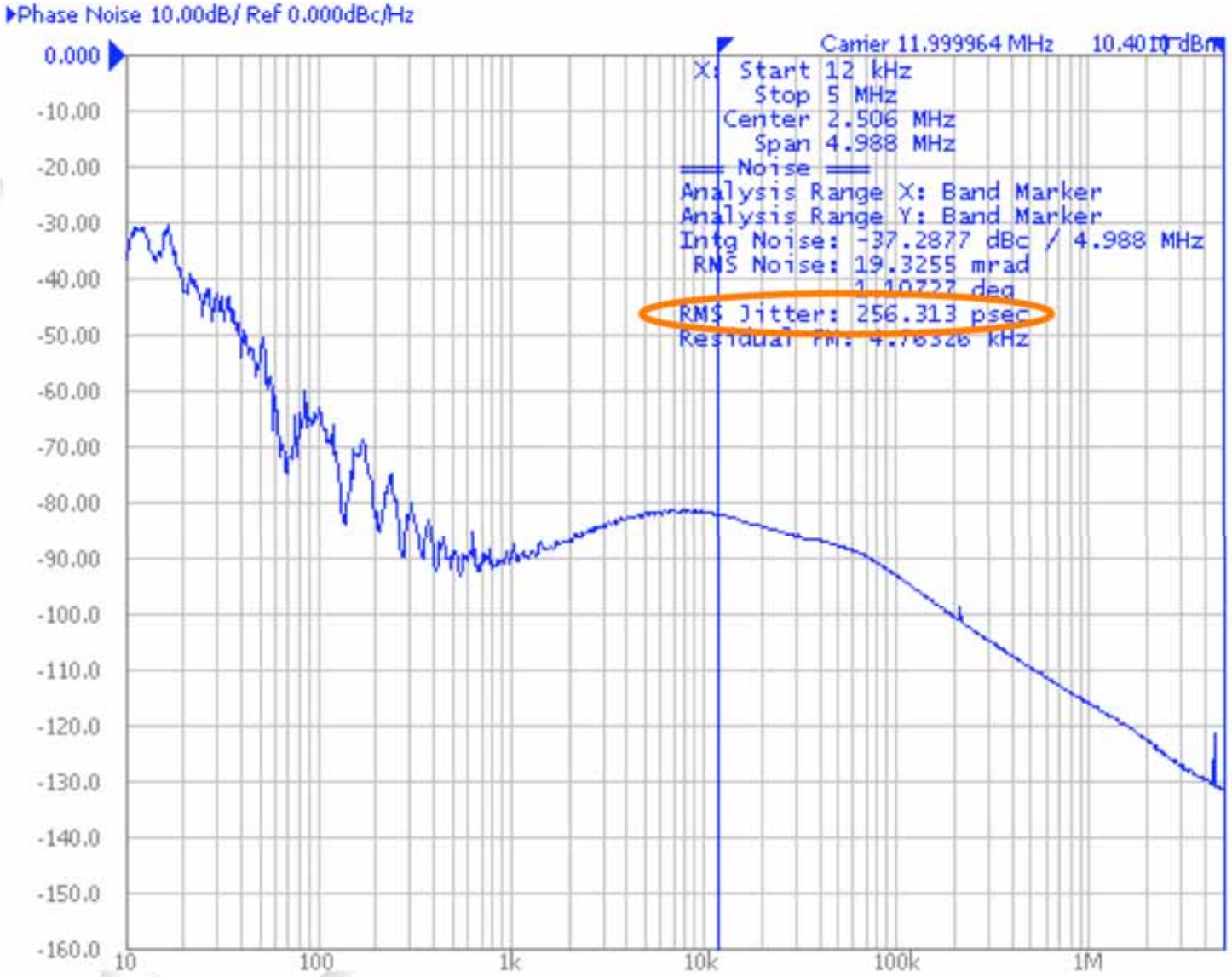
Brick wall filter

EPSON

24MHz XO

0.24ps

RMS phase jitter (12kHz to 5MHz)

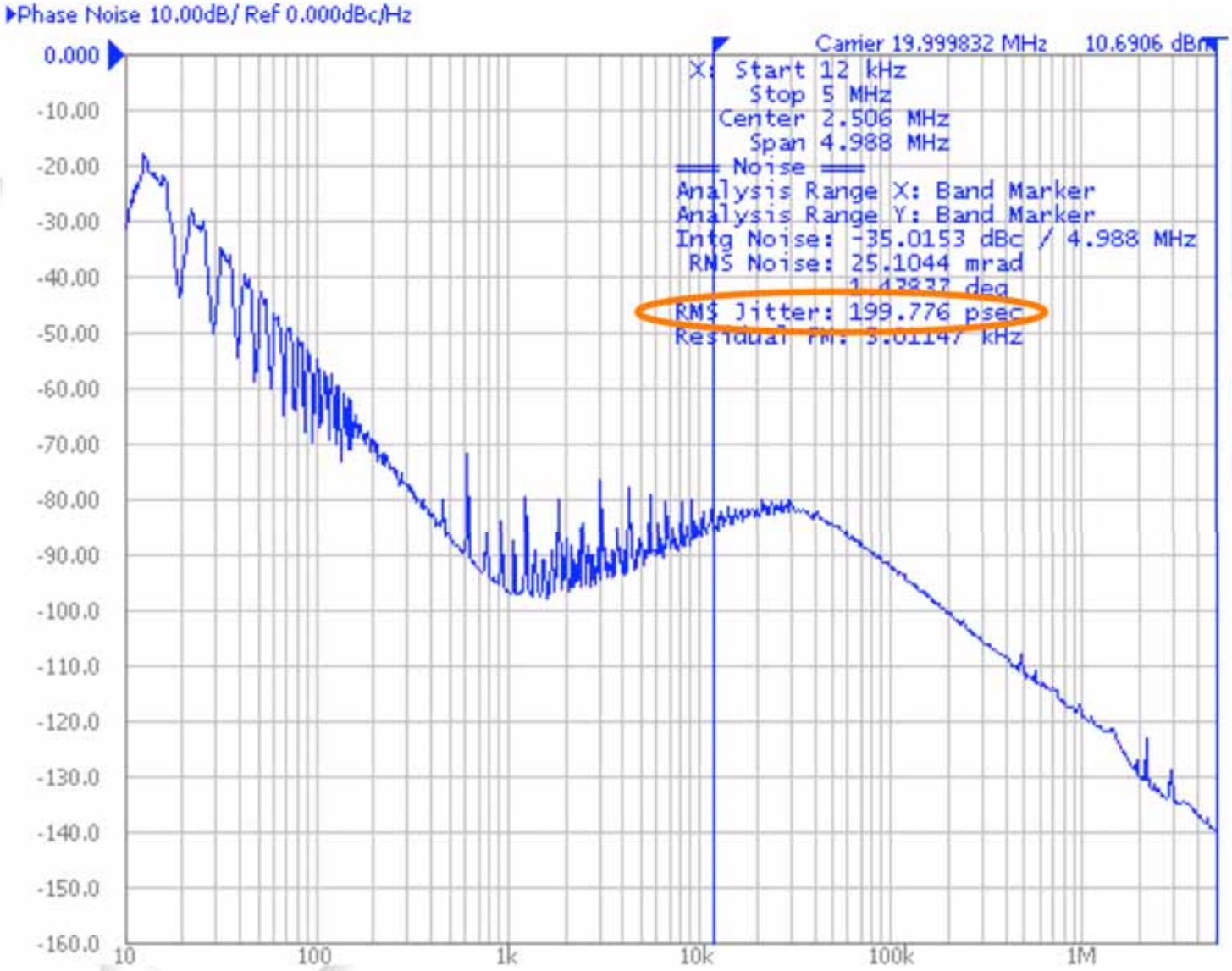


Discera micro communication technologies.

12MHz MEMS-PLL

256ps

RMS phase jitter (12kHz to 5MHz)

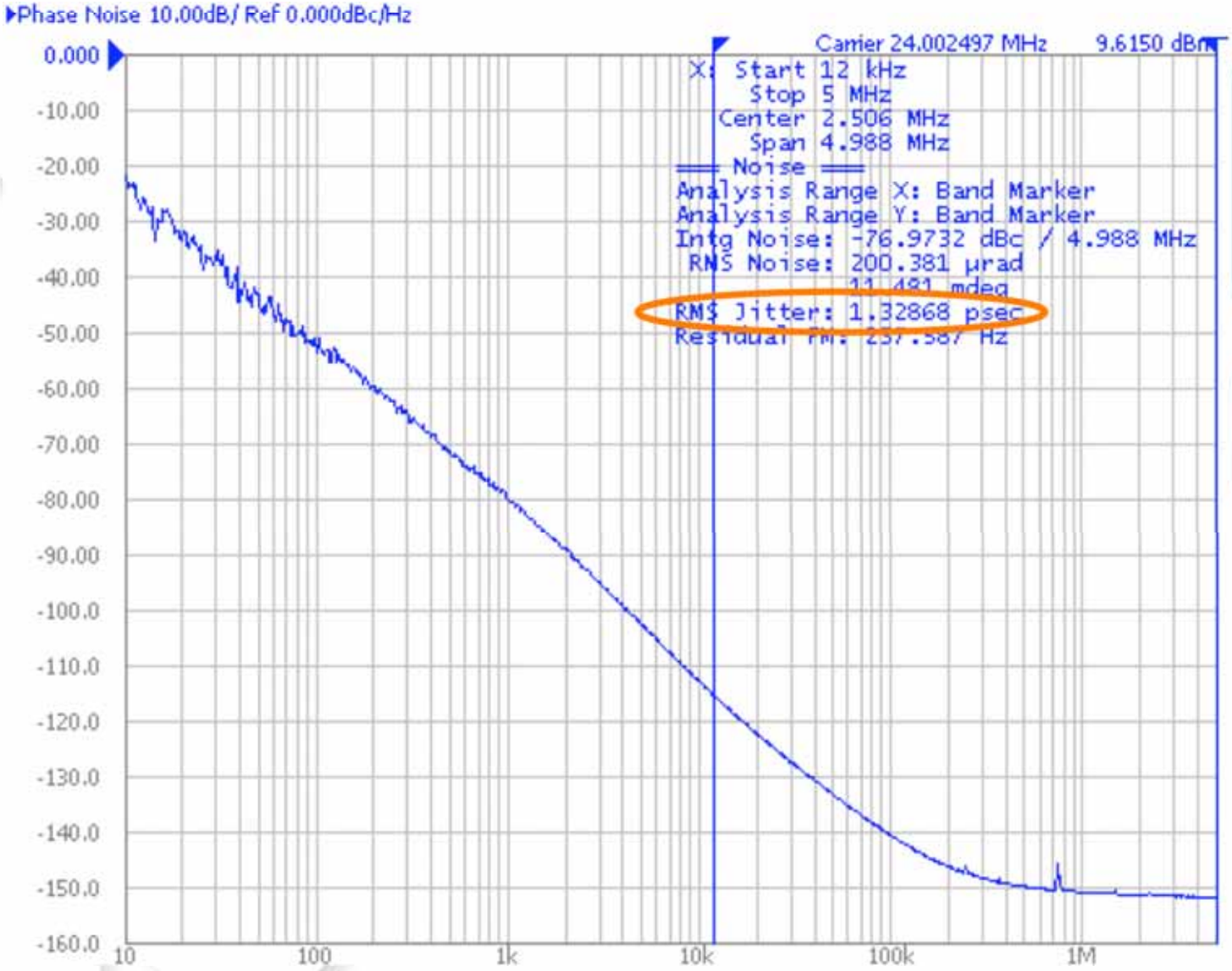


SiTime

20MHz MEMS-PLL

199ps

RMS phase jitter (12kHz to 5MHz)

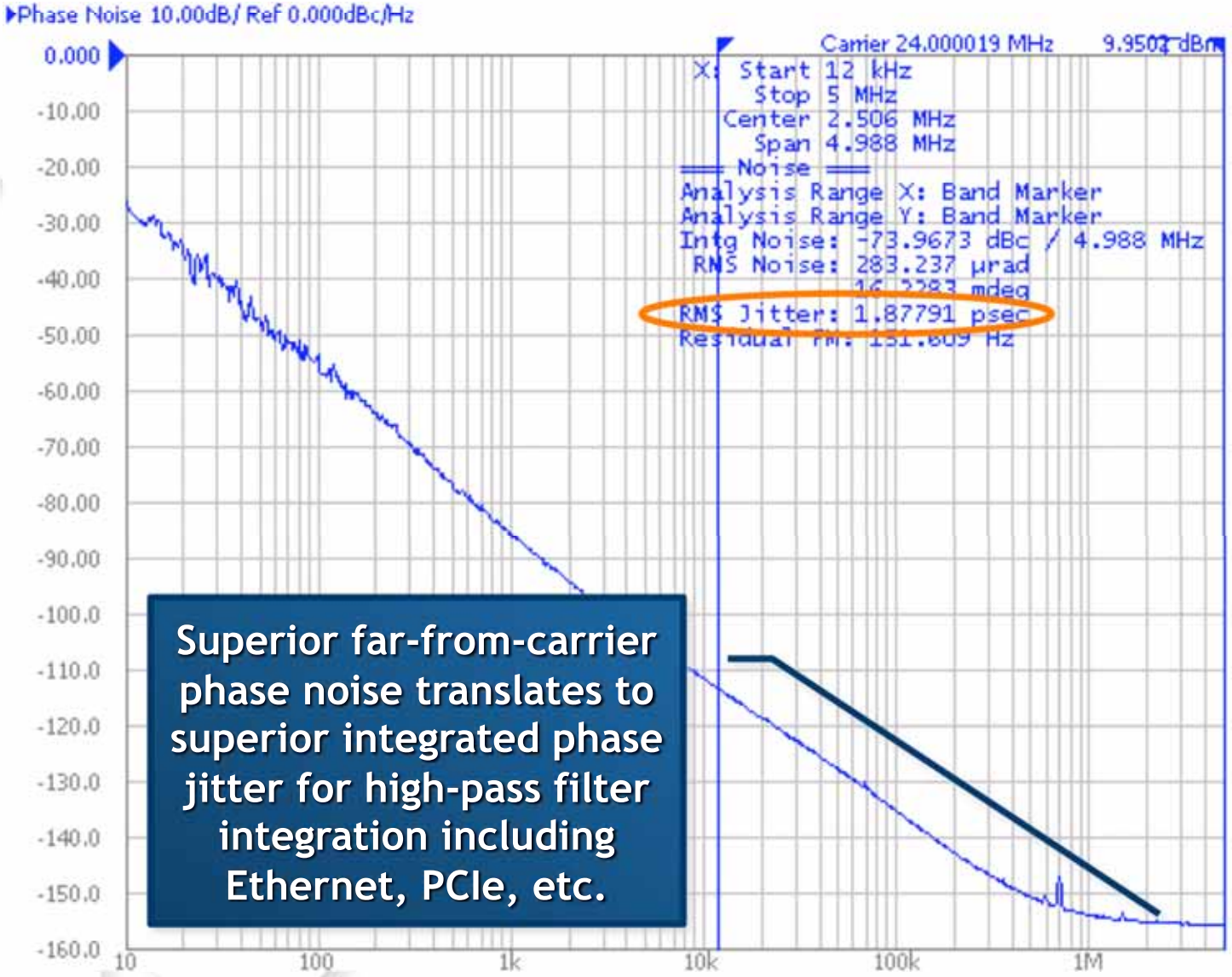


SILICON LABS

24MHz CMOS

1.33ps

RMS phase jitter (12kHz to 5MHz)



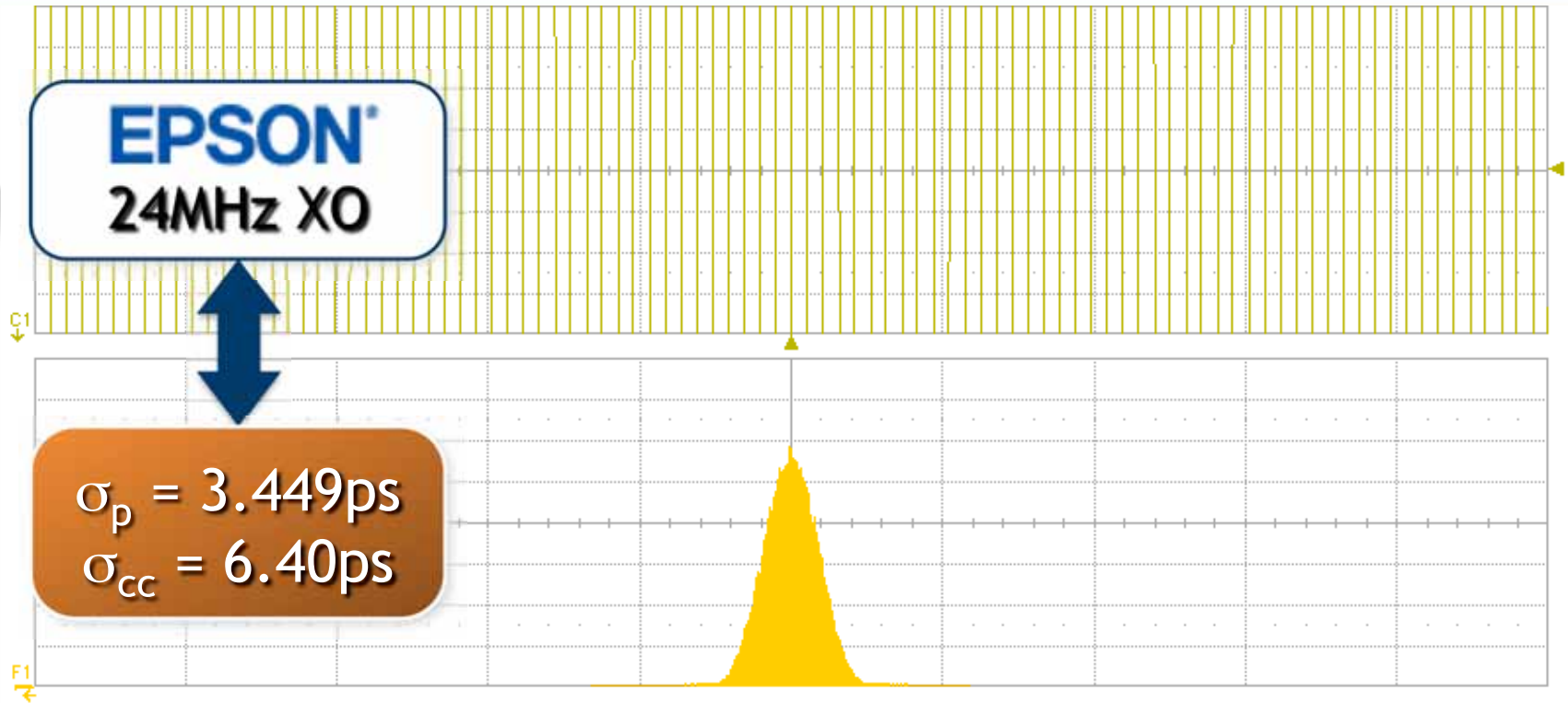
Superior far-from-carrier phase noise translates to superior integrated phase jitter for high-pass filter integration including Ethernet, PCIe, etc.

Mobius Microsystems

24MHz CMOS

1.88ps

RMS period and c-c jitter



Measure	P1:per@lv(C1)	P2:dper@lv(C1)	P3:- - -	P4:- - -	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	41.669 ns	4 ps						
mean	41.66785 ns	0 fs						
min	41.654 ns	-26 ps						
max	41.683 ns	26 ps						
sdev	3.49 ps	6.40 ps						
num	200.836e+3	196.470e+3						
status	✔	✔						

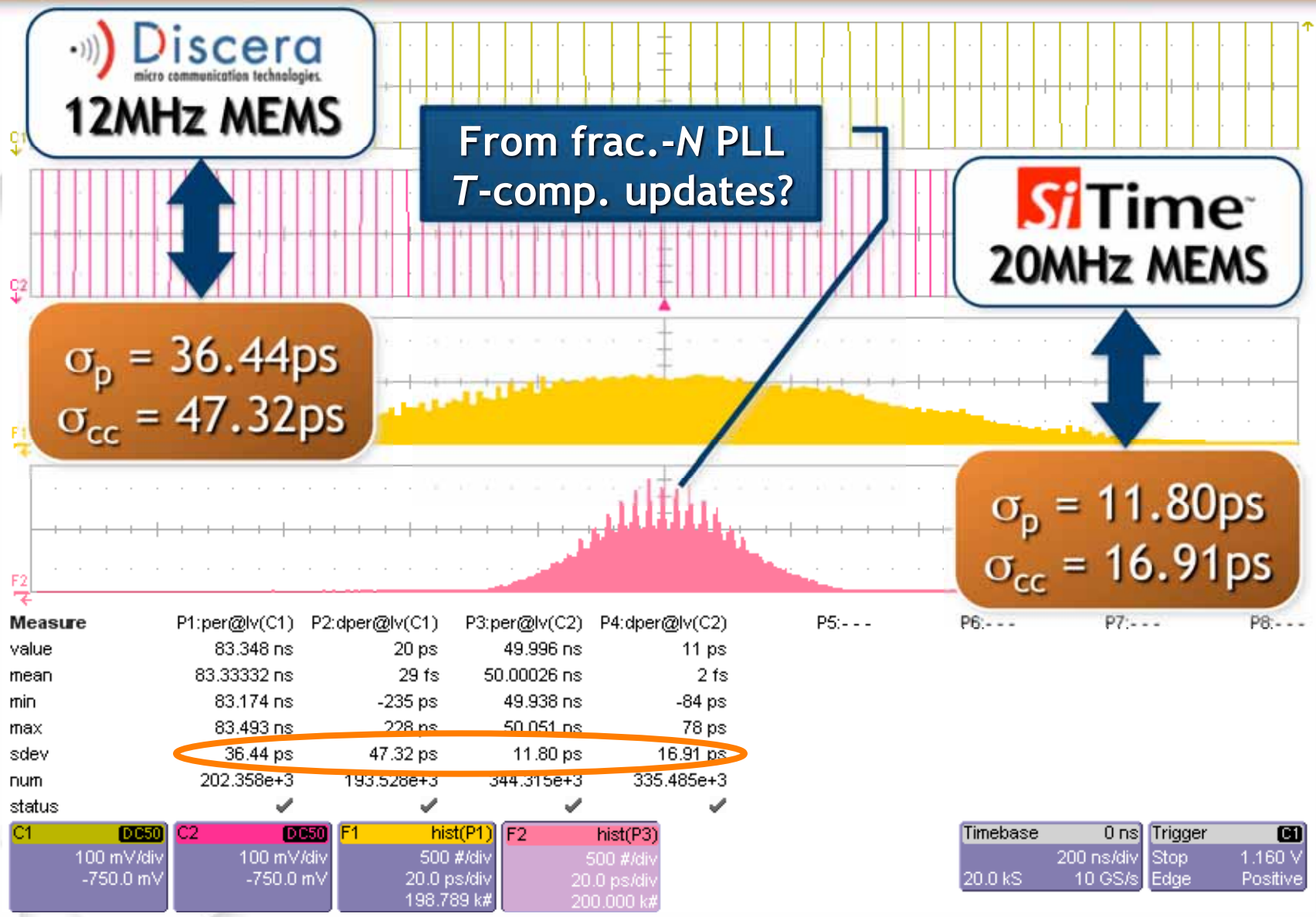
C1 DC50 | 100 mV/div | -750.0 mV

F1 hist(P1) | 400 #/div | 20.0 ps/div | 200.000 k#

Timebase 0 ns | 200 ns/div | 20.0 kS | 10 GS/s

Trigger C1 | Stop 750 mV | Edge Positive

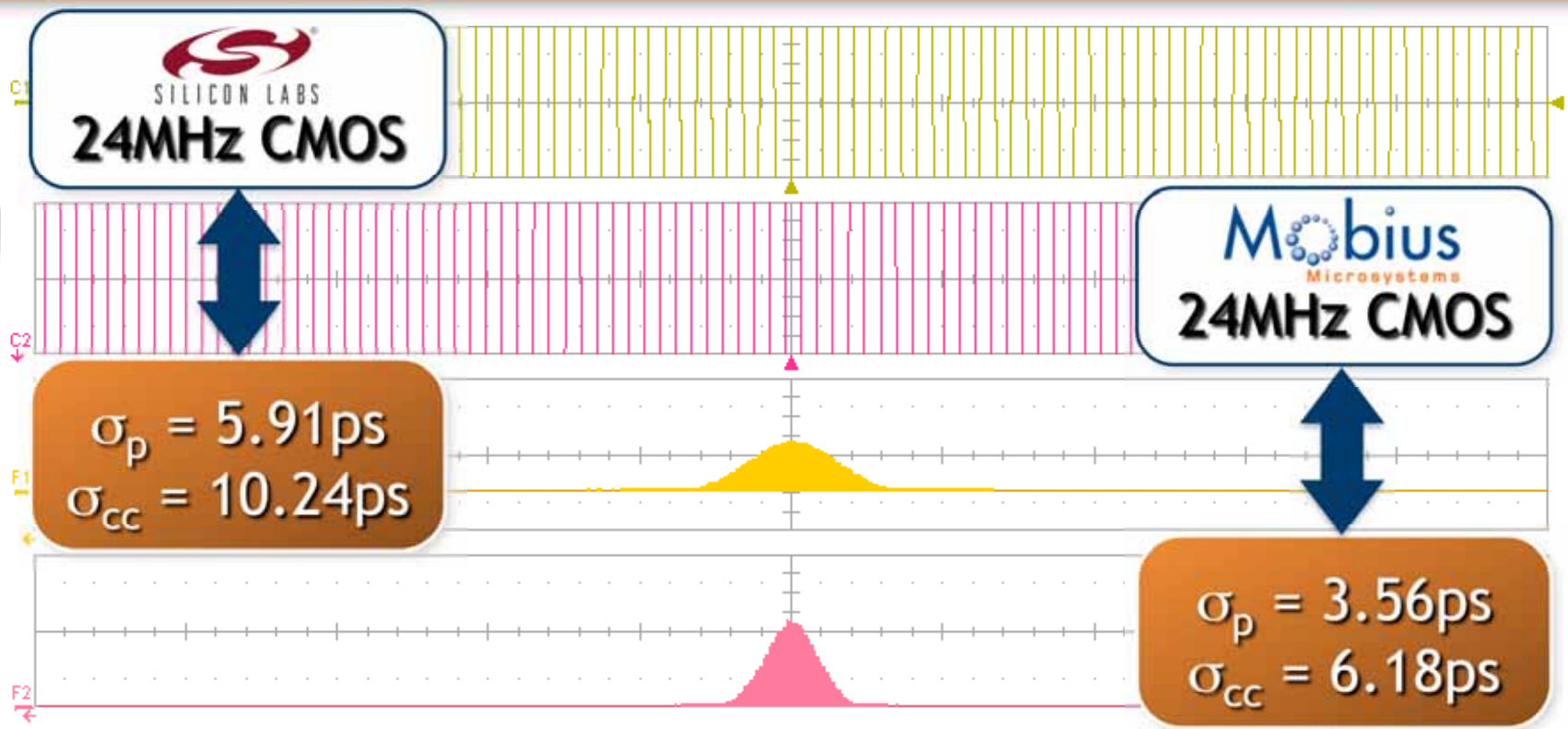
RMS period and c-c jitter



Measure	P1:per@lv(C1)	P2:dper@lv(C1)	P3:per@lv(C2)	P4:dper@lv(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	83.348 ns	20 ps	49.996 ns	11 ps				
mean	83.33332 ns	29 fs	50.00026 ns	2 fs				
min	83.174 ns	-235 ps	49.938 ns	-84 ps				
max	83.493 ns	228 ps	50.051 ns	78 ps				
sdev	36.44 ps	47.32 ps	11.80 ps	16.91 ps				
num	202.358e+3	193.528e+3	344.315e+3	335.485e+3				
status	✔	✔	✔	✔				

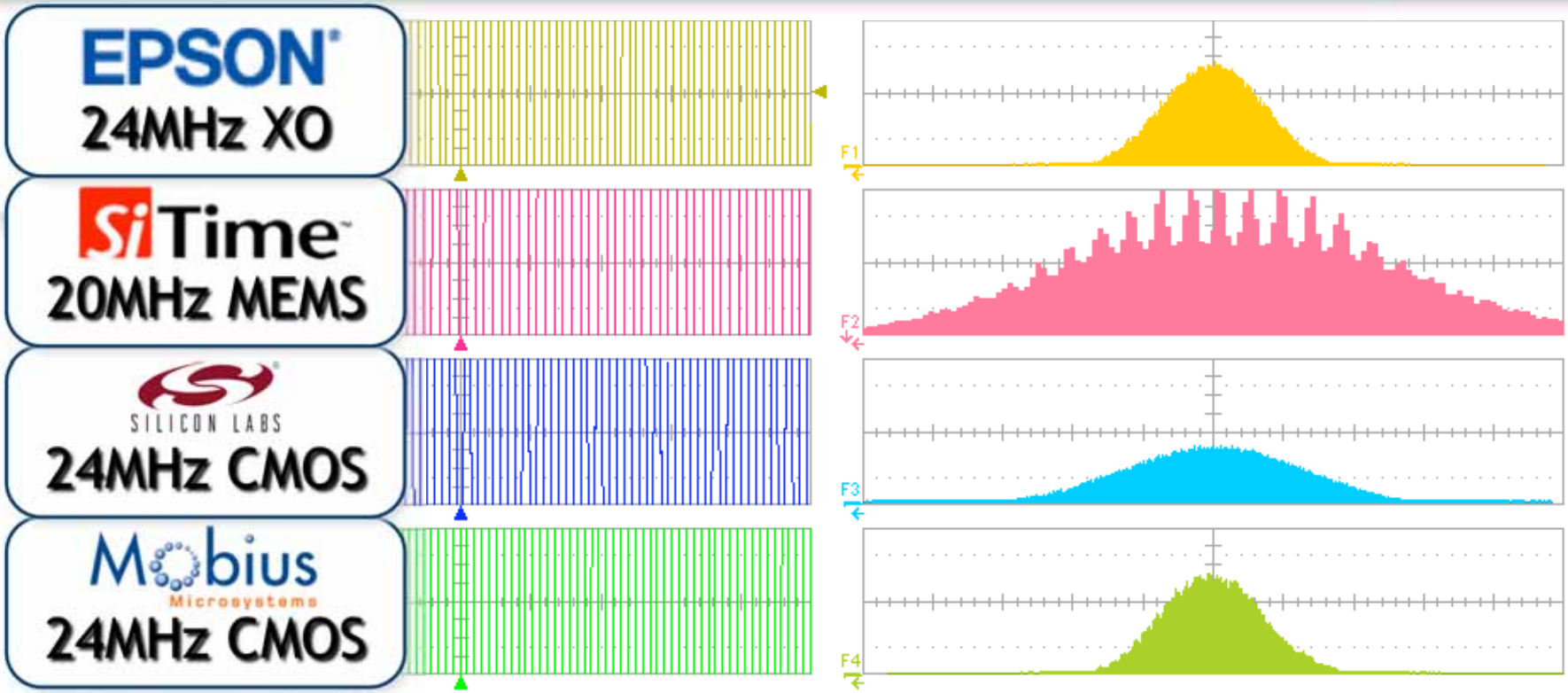
C1 DC50	C2 DC50	F1 hist(P1)	F2 hist(P3)	Timebase 0 ns	Trigger C1
100 mV/div	100 mV/div	500 #/div	500 #/div	200 ns/div	Stop 1.160 V
-750.0 mV	-750.0 mV	20.0 ps/div	20.0 ps/div	20.0 kS 10 GS/s	Edge Positive
		198.789 k#	200.000 k#		

RMS period and c-c jitter



Measure	P1:per@lv(C1)	P2:dper@lv(C1)	P3:per@lv(C2)	P4:dper@lv(C2)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	41.661 ns	-6 ps	41.664 ns	8 ps				
mean	41.66233 ns	2 fs	41.66102 ns	-0 fs				
min	41.635 ns	-48 ps	41.646 ns	-23 ps				
max	41.688 ns	44 ps	41.675 ns	27 ps				
sdev	5.91 ps	10.24 ps	3.56 ps	6.18 ps				
num	200.514e+3	196.155e+3	204.870e+3	200.511e+3				
status	✔	✔	✔	✔				

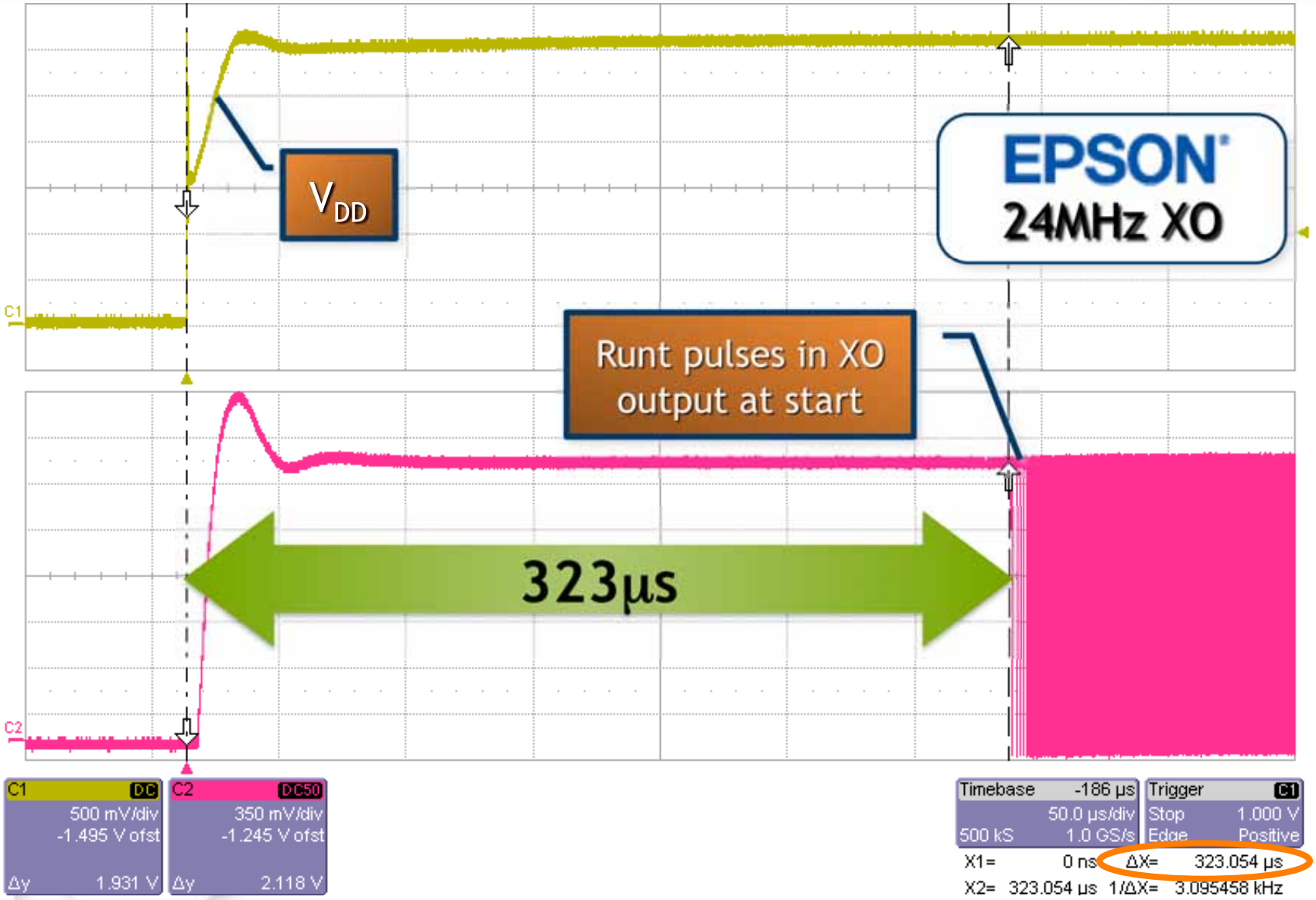
RMS period and c-c jitter



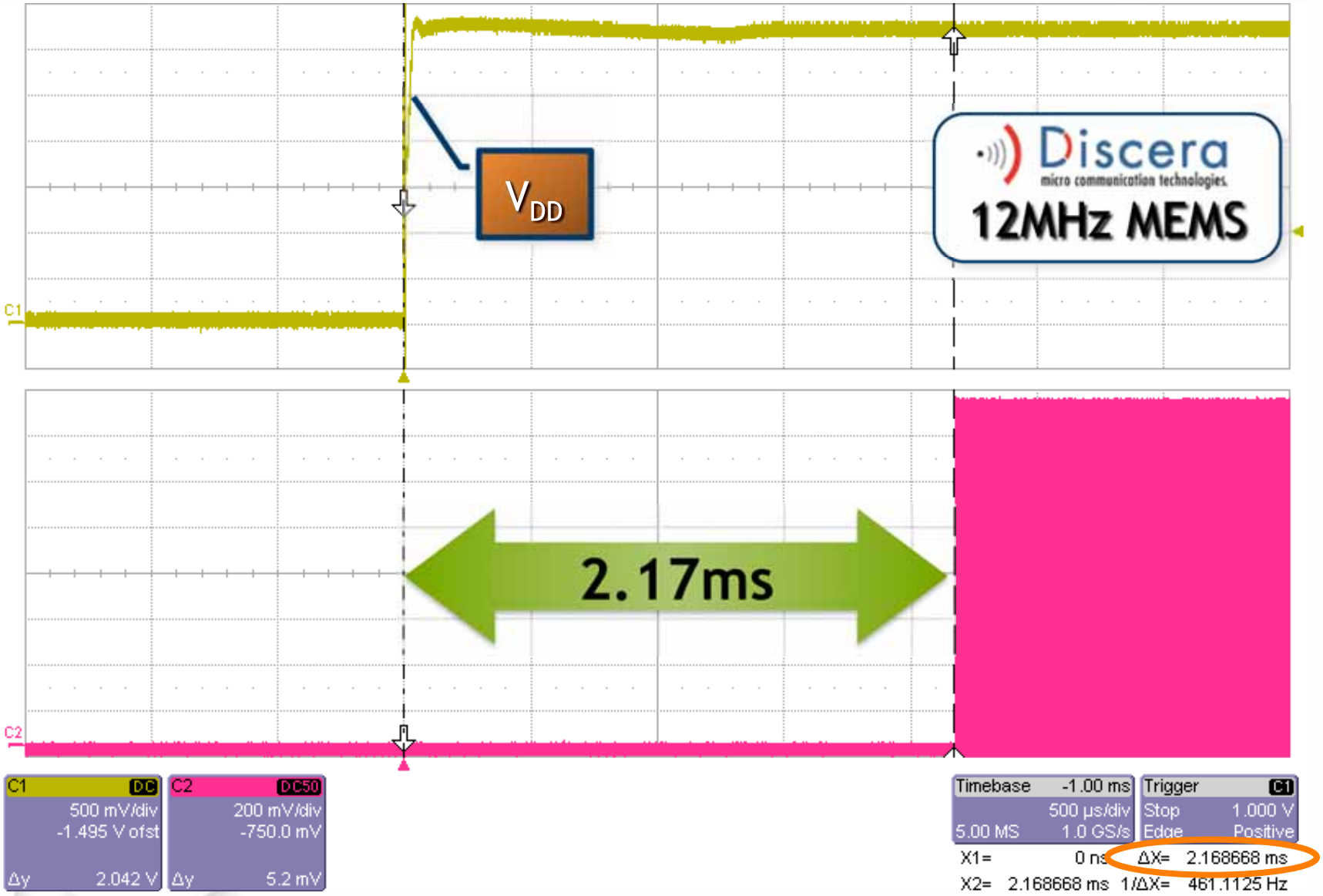
Measure	P1:per@lv(C1)	P2:dper@lv(C1)	P3:per@lv(C2)	P4:dper@lv(C2)	P5:per@lv(C3)	P6:dper@lv(C3)	P7:per@lv(C4)	P8:dper@lv(C4)
value	41.670 ns	2 ps	50.008 ns	22 ps	41.663 ns	4 ps	41.657 ns	-7 ps
mean	41.66785 ns	-2 fs	50.00052 ns	3 fs	41.66237 ns	-1 fs	41.66102 ns	-0 fs
min	41.654 ns	-26 ps	49.947 ns	-85 ps	41.635 ns	-107 ps	41.647 ns	-28 ps
max	41.682 ns	26 ps	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	24 ps
sdev	3.48 ps	6.37 ps	11.77 ps	16.86 ps	6.36 ps	10.33 ps	3.64 ps	6.26 ps
num	245.226e+3	239.895e+3	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	245.220e+3
status	✔	✔	✔	✔	✔	✔	✔	✔

C1 D50	C2 D50	C3 D50	C4 D50	F1 hist(P1)	F2 hist(P3)	F3 hist(P5)	F4 hist(P7)	Timebase 0 ns	Trigger C1
100 mV	100 mV	100 mV	100 mV	400 #	400 #	400 #	400 #	200 ns/div	Stop 750 mV
-750 mV	-750 mV	0.0 mV	-750 mV	5.0 ps	5.0 ps	5.0 ps	5.00 ps	20.0 kS 10 GS/s	Edge Positive
				200 k#	193 k#	200 k#	200 k#		

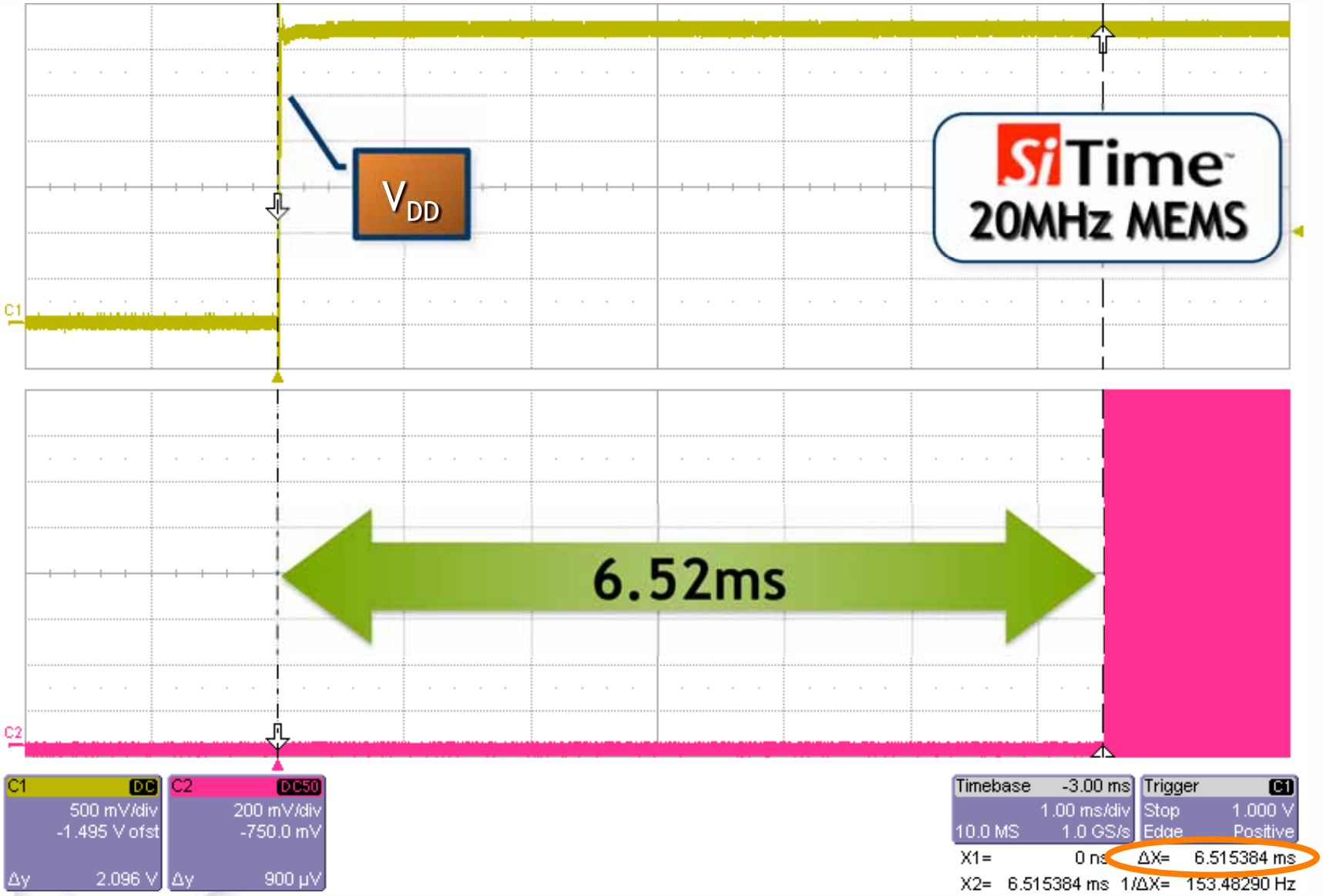
Start-up latency



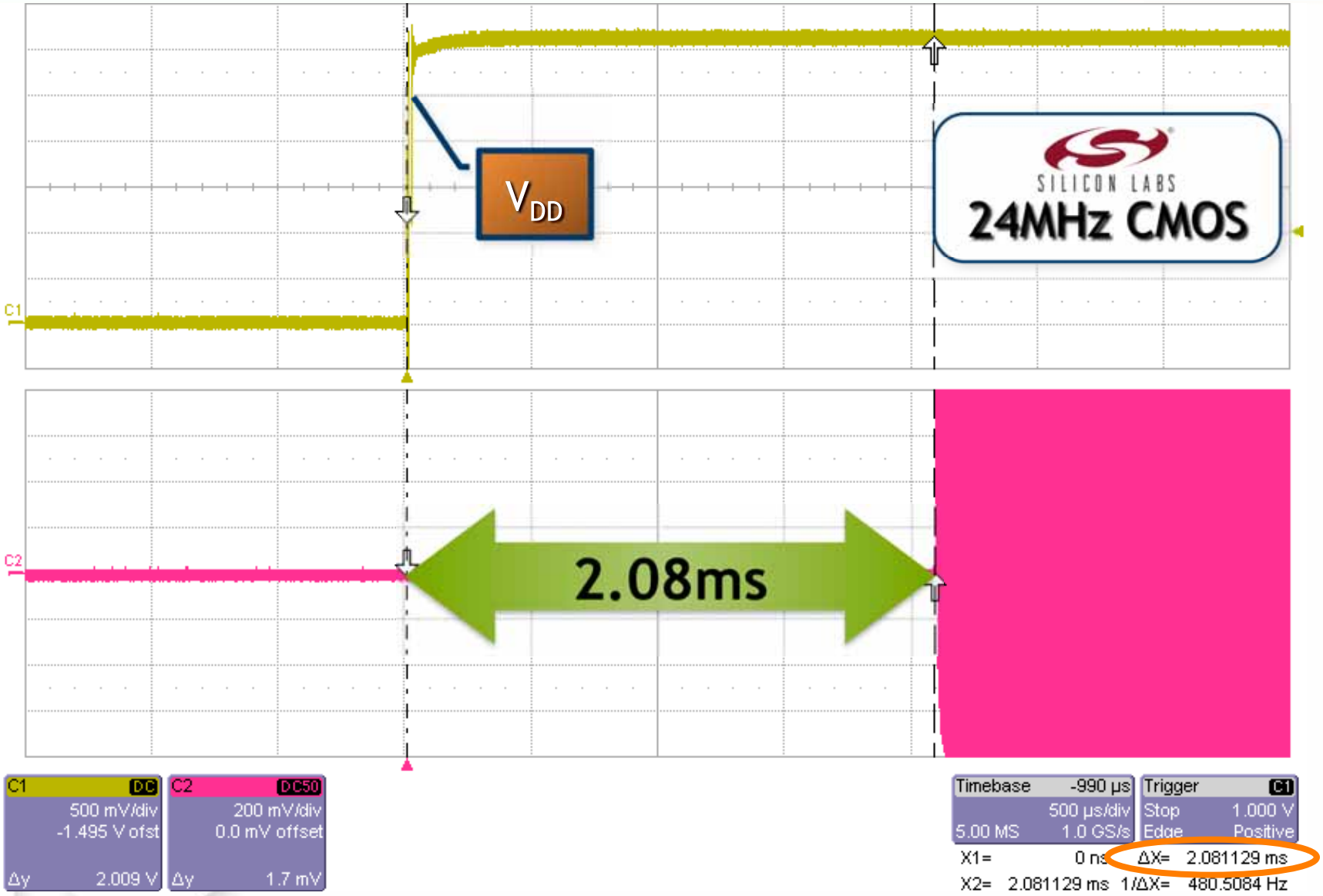
Start-up latency



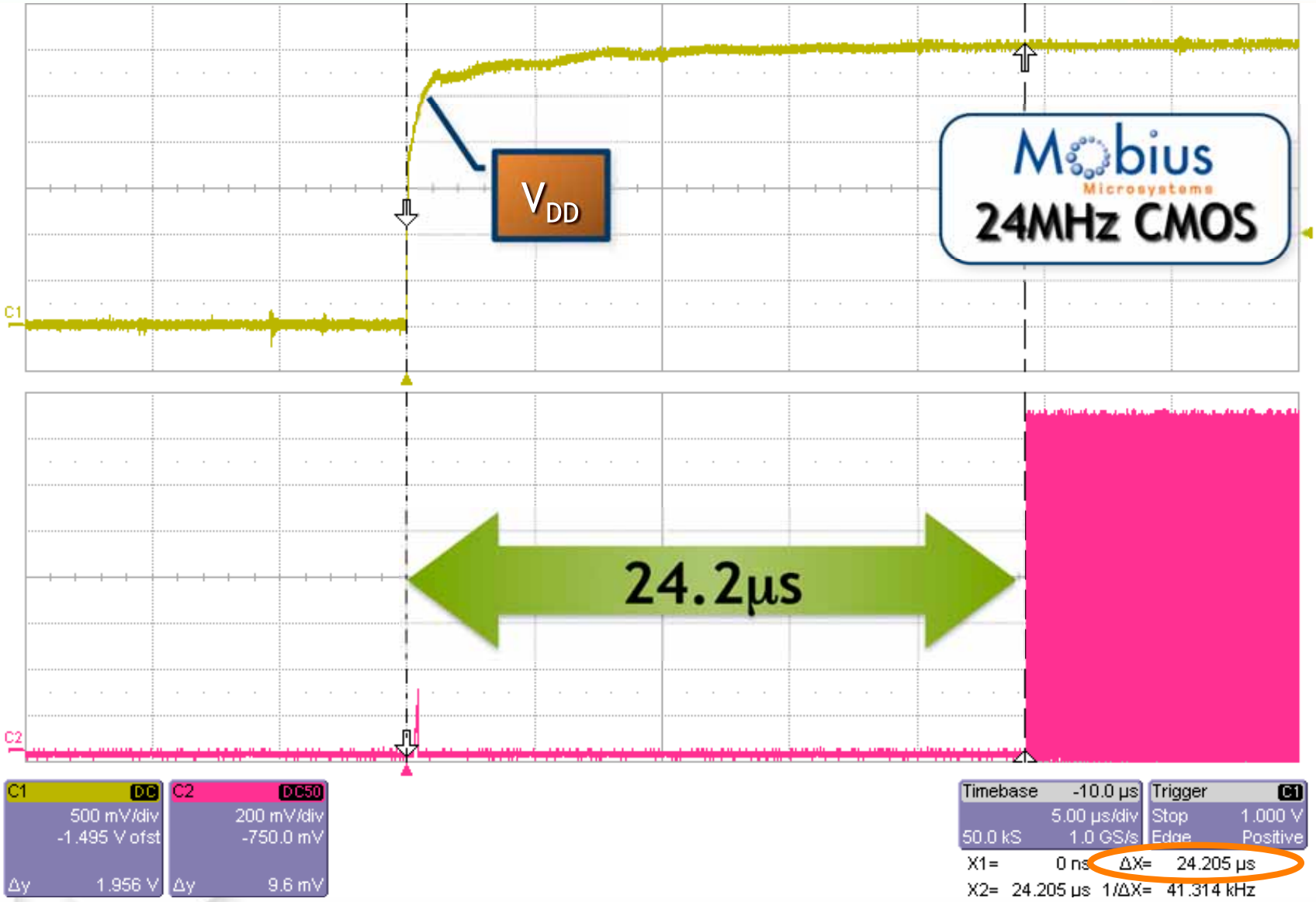
Start-up latency



Start-up latency



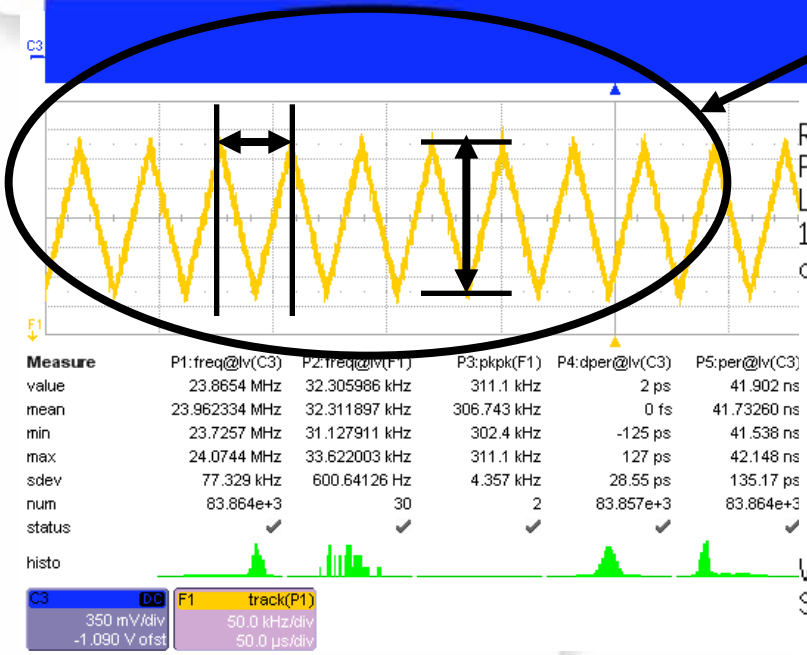
Start-up latency



Spread spectrum clock generation

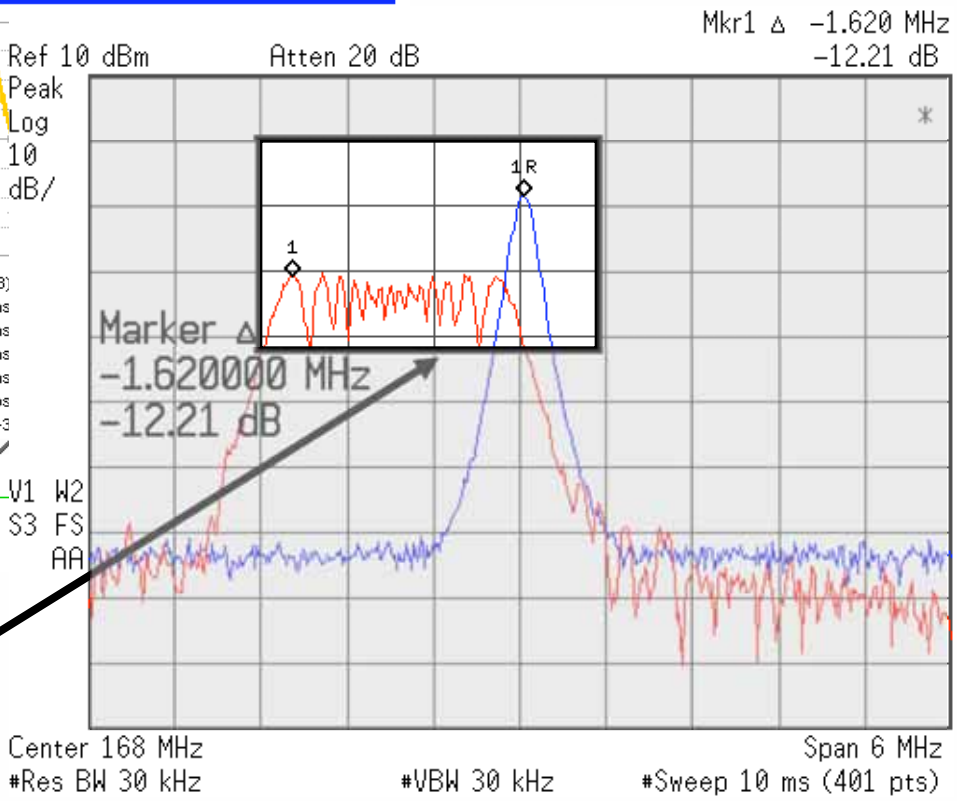
Mobius Microsystems

Mobius Microsystems
24MHz CMOS



Time domain clock signal

24MHz, 32kHz, -1%



12.2dB

7th Harmonic Peak Power Reduction

Summary of measured performance

Mobius Microsystems

Metric	*XO (Epson)	*MEMS (Discera)	*MEMS (SiTime)	*CMOS (SiLabs)	CMOS (Mobius)
Frequency (MHz)	24	12	20	24	24
Worst case frequency error from -20-90C (ppm)	9	10	50	53	54
SSB phase noise (dBc/Hz) @ 10Hz/100Hz 1kHz/10kHz 100kHz/1MHz	-91/-119 -129/-148 -154/-162	-28/-62 -90/-82 -93/-116	-29/-54 -95/-86 -93/-119	-24/-53 -80/-113 -141/-151	-24/-56 -86/-112 -135/-154
RMS phase jitter integrated from 12kHz to 5MHz (ps)	0.24	256	199	1.33	1.88
RMS period/c-c jitter (ps)	3.48/6.37	36.44/47.32	11.77/16.86	6.36/10.33	3.64/6.26
Start-up latency (ms)	0.323	2.17	6.52	2.08	0.0242
Unloaded V_{DD}/I_{DD} (V/mA)	3.3/2.8	3.3/3.2	3.3/13.8	3.3/13.1	3.3/3.0
Unloaded power (mW)	9.2	10.6	45.5	43.2	9.9

*These are devices that are currently available via distribution channels; devices exhibiting better performance may exist

Summary of measured performance

Mobius Microsystems

Metric	*XO (Epson)	*MEMS (Discera)	*MEMS (SiTime)	*CMOS (SiLabs)	CMOS (Mobius)
Frequency (MHz)	24	12	20	24	24
Worst case frequency error from -20-90C (ppm)	**9**	**10**	50	53	54
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Summary

- None of the emerging frequency generators directly rival quartz on all metrics
- CMOS implementations offer:
  - Lowest phase noise (despite much lower *Q*)
  - Lowest jitter (integrated and period)
  - Integration potential (standard CMOS)
  - A single die frequency generator
  - Low power (*Mobius* implementation)
  - Highest functionality
- MEMS implementations generally offer:
  - Slightly better frequency accuracy
  - Low power (*Discera* implementation)

APPLICATIONS, FUTURE TRENDS AND CONCLUSION

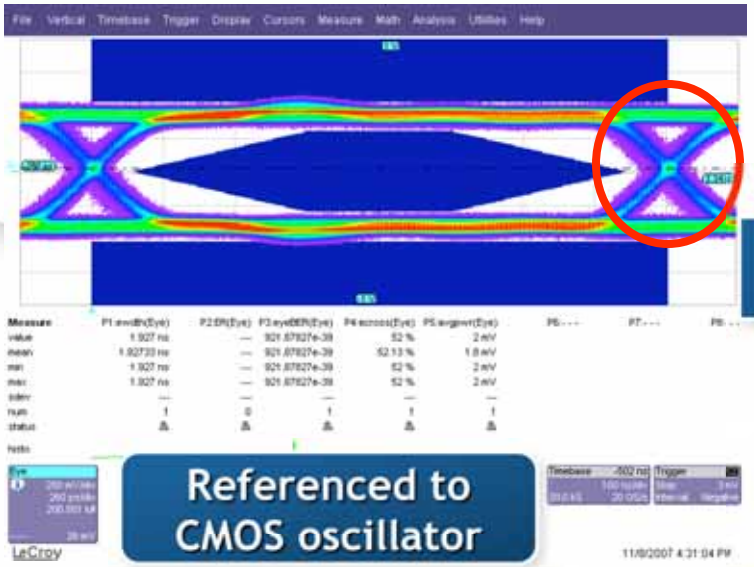
Applications: Wireline

Thin and Portable

CMOS oscillators

- Wireline: well-suited
  - 100 – 500ppm
  - Jitter determines BER
  - Low power
  - High frequency
  - Replace channel-rate PLL?
- Many interfaces
  - USB, S-ATA, PCIe, Ethernet
- Requirements
  - Low-profile
  - Low-cost
  - Low-power
  - High-reliability

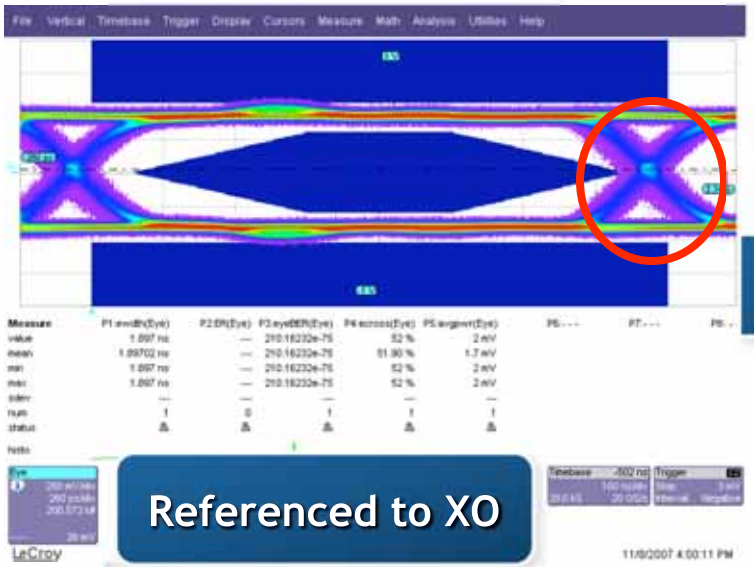
Applications: Wireline (USB)



Referenced to CMOS oscillator

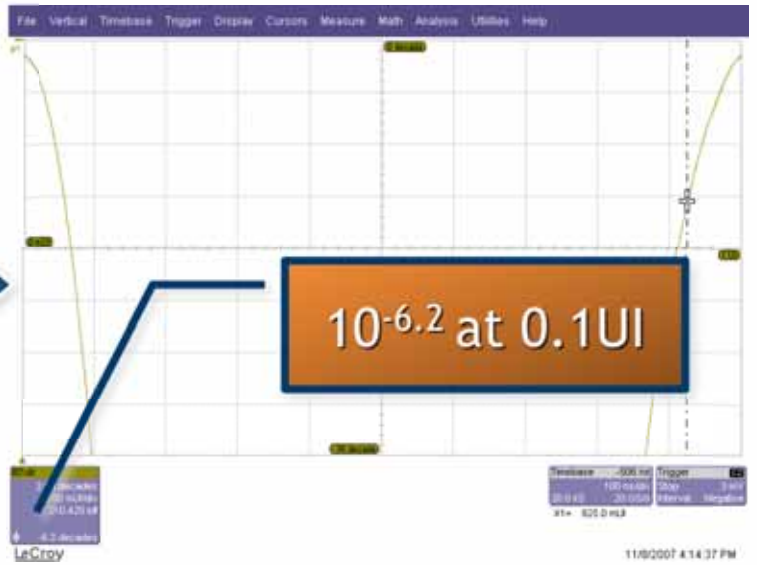
CMOS

CMOS oscillator exhibits substantially better BER



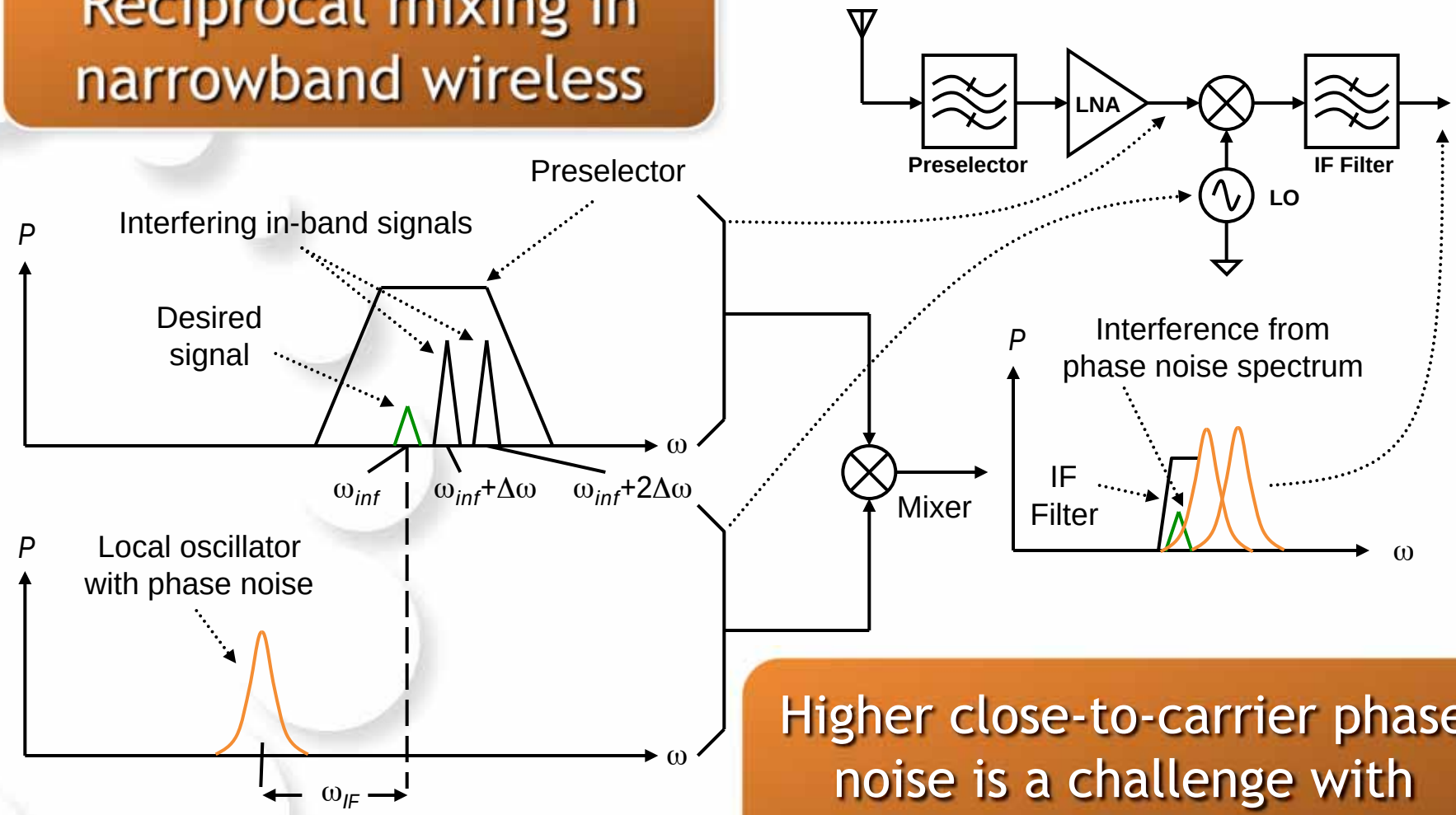
Referenced to XO

XO



Applications: Wireless

Reciprocal mixing in narrowband wireless



Higher close-to-carrier phase noise is a challenge with CMOS and MEMS oscillators

Applications: Wireless

Mobius Microsystems

Wideband Com.

WiMedia ALLIANCE

TPMS

CMOS oscillators

- Narrowband: not suited
  - Reciprocal mixing
  - Served by TCXO (<5ppm)
- Wideband: well-suited
  - Looser accuracy
  - High-frequency
  - Low start-up latency
  - Low-power
- Other applications?

Future trends

- On CMOS oscillators
  - Advances in RF-CMOS will enable better CMOS oscillators
  - CMOS oscillators are challenging to develop, but offer the best performance, form-factor and cost
- CMOS vs. MEMS
  - MEMS is likely to continue to scale to better accuracies than CMOS oscillators
  - BUT, CMOS oscillators are ~10 years behind MEMS in development
- Quartz
  - Quartz will not be displaced *en masse*
  - Emerging technologies complement existing frequency generation products, particularly against dimensions where quartz no longer scales

Conclusions

- Frequency generation has been an exciting technical space for well over 100 years (and particularly in the past 5-10 years)
- Limitations in quartz scaling are nearing and market demands are beyond scaling limits
- New technologies, such as CMOS and MEMS oscillators do not rival quartz on all dimensions
- The presented CMOS oscillators offer the best overall performance in a standard integrated platform

QUESTIONS WELCOME

Speaker biography

Dr. Michael McCorquodale is the founder and CTO of *Mobius Microsystems*, which was founded based on his research in precision solid-state and MEMS oscillators. On that work, Michael has published over 20 technical articles, presented at over 25 academic and industry conferences and holds inventorship on over 25 issued and pending U.S. patents. Michael earned the B.S.E. degree with honors from the University of Illinois at Urbana-Champaign and the M.S.E and Ph.D. degrees from the University of Michigan, all in electrical engineering. While at the University of Michigan, Michael received the Distinguished Electrical Engineer Award, the Harry B. Benford Entrepreneurial Leadership Award and was the sole national recipient of the Armed Forces Communications and Electronics Association Doctoral Fellowship in 2002. He has also served as an adjunct faculty member at the University of Michigan in the department of Electrical and Computer Engineering.